Question Paper Code

11485

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

Sixth Semester

Electrical and Electronics Engineering

(Common to Seventh Semester - Electronics and Instrumentation Engineering)

EE8691 - EMBEDDED SYSTEMS

(Regulations 2017)

Duration: 3 Hours

Max. Marks: 100

$PART - A (10 \times 2 = 20 Marks)$

Answer ALL Questions

	THIS WEITTED QUESTIONS			
1.	Give some examples for small scale embedded systems.	Marks, K-Level, CO 2,K1,CO1		
2.	Define device driver.	2,K1,CO1		
3.	What is a CAN bus? Where is it used?	2,K2,CO2		
4.	What is meant by UART?	2,K1,CO2		
5.	Illustrate state machine model.	2,K1,CO3		
6.	What are queue and stack?	2,K1,CO3		
7.	Define Semaphore.	2,K1,CO4		
8.	List the functions of a kernel.	2,K1,CO4		
9.	Identify the importance of temperature and level sensor in washing machine.	2,K1,CO5		
10.	Comment on charge pump circuit in smart card.	2,K2,CO5		
PART - B (5 × 13 = 65 Marks) Answer ALL Questions				

11.	a)	Explain the hardware units of embedded system.
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(i)Memory	
	3,K2,C01
(ii)Watch dog timer	5,K2,CO1
(iii)Input and output port	5,K2,CO1

OR

b) Discuss in detail design process in embedded system.

13,K2,CO1

12. a) Describe one type of serial communication bus with its communication 13,K2,CO2 protocol.

OR

b)	Describe about RS4	85 protocol and	differentiate it with RS232.
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13,K2,CO2

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

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13.	a)	Illustrate about the linear or waterfall model in embedded system.	13,K2,CO3
		OR	
	b)	Discuss the sequential model program with example.	13,K2,CO3
14.	a)	Explain Task communication, shared memory and message passing.	13,K2,CO4
		OR	
	b)	Discuss Inter Process Communication and context switching.	13,K2,CO4
15.	a)	Explain about the concept of embedded system in ATM machine.	13,K2,CO5
		OR	
	b)	With suitable diagram, discuss the concept of smart card system application in embedded system.	13,K2,CO5
		$PART - C (1 \times 15 = 15 \text{ Marks})$	
16.	a)	With neat diagram, explain the working of direct memory access architecture and timing diagram. OR	15,K2,CO1
	b)	Elaborate Semaphores, Mailbox, Pipes and shared memory in RTOS.	15,K2,CO4