15 FEB 2023

Reg. No.													

Question Paper Code	11719

B.E./B.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

Third Semester

Electrical and Electronics Engineering

20EEPC304 - DIGITAL LOGIC CIRCUITS

(Regulation 2020)

Duration: 3 Hours | Max. Marks: 100

PART-A (10 × 2 = 20 Marks)

Answer ALL Questions

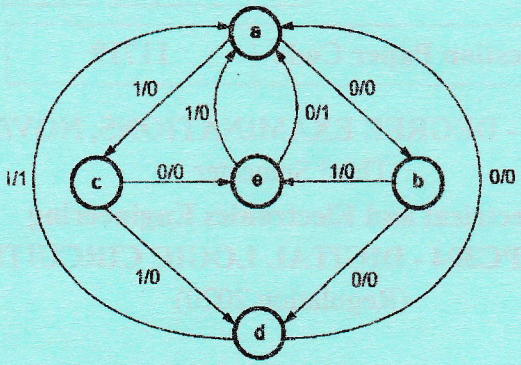
		Marks, K-Level, CO
1.	Construct AND and OR gates using NAND gates.	2,K2,CO1
2.	List the advantages of CMOS.	2,K1,CO1
3.	Define Combinational Logic Circuits with example.	2,K1,CO2
4.	Draw the symbol of 2:1 MUX.	2,K1,CO2
5.	Compare Level Triggering and Edge Triggering.	2,K2,CO3
6.	State the rules for State Assignment.	2,K1,CO3
7.	Define Race condition.	2,K1,CO4
8.	List the analysis procedure of asynchronous sequential circuits.	2,K1,CO4
9.	Compare PLA and PAL.	2,K1,CO5
10.	What are the advantages of hardware languages?	2,K1,CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	(i) Encode a binary word 1011 into seven bit even parity Hamming code.	08,K3,CO1
		(ii) Convert $(0.6875)_{10}$ to its equivalent binary.	02,K3,CO1
		(iii) Convert hexadecimal number A.14 to its equivalent Octal number.	03,K3,CO1
		OR	
	b)	Explain the working of TTL and ECL logic families.	13,K2,CO1
12.	a)	(i) Express F=A+B'C in Canonical SOP and Canonical POS form.	07,K2,CO2
		(ii) Simplify using K-Map F(A,B,C,D)= ∑m(0,2,3,6,7)+d(8,10,11,15).	06,K3,CO2
		OR	
	b)	Design a 4 bit Gray to Binary Code Converter.	13,K3,CO2
13.	a)	Explain SR and D flip flop with necessary diagrams, state diagram, truth table, characteristics equation and excitation table.	13,K2,CO3
		OR	

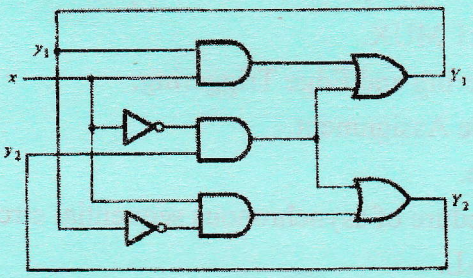
b) Design a sequential circuit for the following state diagram. *13,K3,CO3*



14. a) Explain Hazards and its types. Implement the Boolean function $F(A,B,C,D)= \sum m(0,2,6,7,8,10,12)$ without static hazard. *13,K3,CO4*

OR

b) Analyze the given asynchronous sequential diagram and draw maps, transition table and state table. *13,K3,CO4*



15. a) (i) Implement the following functions using PLA. *08,K3,CO5*
$F_1= \sum m(1,2,4,6)$, $F_2= \sum m (0,1,6,7)$ & $F_3= \sum m(2,6)$

(ii) Explain in detail about FPGA. *05,K2,CO5*

OR

b) Write a VHDL code for full adder in Behavioral and structural Model. *13,K2,CO5*

PART C (1 × 15 = 15 Marks)

16. a) Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. *15,K3,CO4*

OR

b) Develop an asynchronous sequential circuit with 2 inputs X and Y and with one output Z. whenever Y is 1 , input X is transferred to Z. When Y is zero, the output does not change for any change in X. Use SR FF for circuit implementation. *15,K3,CO4*