28 FEB 2023

Reg. No.												

Question Paper Code	11737

B.E/B.Tech - DEGREE EXAMINATIONS, NOV/DEC 2022

Semester

Information Technology

(Common to Computer Science and Engineering & M.Tech. - Computer Science and Engineering)

20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Regulations 2020)

Duration: 3 Hours

Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

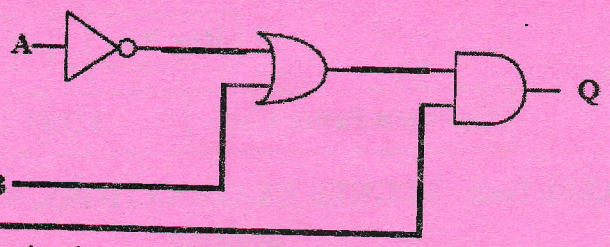
Answer ALL Questions

		Marks, K-Level,CO
1.	Implement AND gate using only NOR gate.	2,K1,CO1
2.	Find the octal and binary equivalent of hexadecimal numbersAB.CD.	2,K1,CO1
3.	Design the combinational circuit with 3 inputs and 1output. The output is 1 when the binary value of the input is less than 3 and the output is 0 otherwise.	2,K2,CO2
4.	Distinguish between combinational logic circuit and sequentiallogic circuit.	2,K2,CO2
5.	Differentiate Mealy circuit and Moore circuit.	2,K2,CO3
6.	Write the characteristics table and excitation table of SR flipflop.	2,K1,CO3
7.	Write the HDL code for Half adder using gate level modeling.	2,K1,CO4
8.	What is Verilog?What are the different types of Modeling?	2,K1,CO4
9.	Compare SRAM and DRAM.	2,K1,CO6
10.	A seven bit Hamming code is received as 1111110.What is the correct code?	2,K1,CO6

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Simplify the following functions using K-map technique (i) G(A,B,C,D)=∑m(0,1,3,7,9,11). (ii) f(w,x,y,z)=∑m(0,7,8,9,10,12)+∑d(2,5,13).	13,K2,CO1
		OR	
	b)	(i) Express the following function in sum of min-terms and product of max-terms F(X,Y,Z)=X+YZ	7,K2,CO1
		(ii) Convert the following logic system into NAND gatesonly.	6,K2,CO1



12. a) Design a logic circuit that accepts a 4 bit Gray code and converts it into 4 bit binary code. *13,K2,CO2*

OR

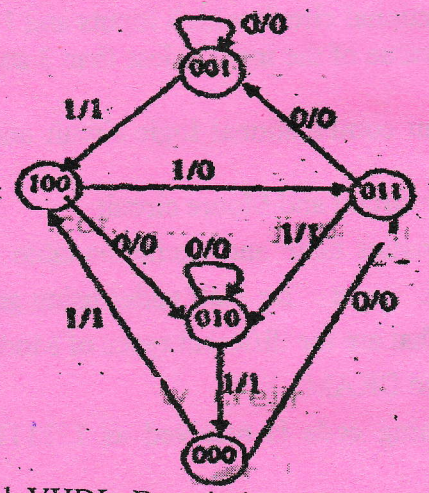
b) (i) Realize 4 x 16 decoder using 3 x 8 decoders with enable input. *6,K2,CO2*

(ii) Implement the following functions using a 4*1 multiplexer. $F(W,X,Y,Z)= \sum m (0,1,3,4,8,9,15)$. *7,K2,CO2*

13. a) Design a modulo 5 synchronous counter using JK Flip Flop and implement it. *13,K2,CO3*

OR

b) Design a sequential circuit by the following state diagram using T-flip flops. *13,K2,CO3*



14. a) Write behavioural VHDL Description of 8 bit shift register with direct reset *13,K2,CO4*

OR

b) Design a 2-bit magnitude comparator and write a verilog HDL code *13,K2,CO4*

15. a) Implement the switching functions. *13,K2,CO6*

Z1=ab'd'e+a'b'c'd'e'+bc+de

Z2=a'c'e

Z3=bc+de+c'd'e'+bd

Z4=a'c'e+ce

using 5 x 8 x 4 PLA

OR

b) Implement the following function using PAL *13,K2,CO6*

F1 (A, B,C) = Σ(1, 2, 4, 6);
F2 (A, B, C) = Σ(0, 1, 6, 7);
F3 (A, B,C) = Σ(1, 2, 3, 5, 7).

PART - C (1 × 15 = 15 Marks)

16. a) Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z Wherever Y is 1, input X is transferred to Z. When Y is 0; the output does not change forany change in X. Use SR latch for implementation of the circuit. *15,K2,CO5*

OR

b) Design an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When second input also becomes 1, z=0; the output stays at 0 until circuit goes back to initial state. *15,K2,CO5*