24 JUL 2023

Reg. No.													

Question Paper Code	12079

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2023

Fourth Semester

Electronics and Instrumentation Engineering

(Common to Instrumentation and Control Engineering)

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Explain parity bit.	*2,K2,CO1*
2.	Summarize the features of emitter coupled logic.	*2,K2,CO1*
3.	Illustrate full adder with truth table and logic diagram.	*2,K2,CO2*
4.	Explain the 8X3 encoder with suitable logic diagram.	*2,K2,CO2*
5.	Compare the level triggering and edge triggering.	*2,K2,CO3*
6.	Relate the timing diagram for clock response in latch and flip-flop.	*2,K2,CO3*
7.	Define PROM.	*2,K1,CO4*
8.	Outline the features of CPLD.	*2,K2,CO4*
9.	Build a VHDL code for 4X1 multiplexer.	*2,K2,CO5*
10.	Model JK flip flop using VHDL code.	*2,K2,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	(i) Convert $(153.513)_{10}$ to octal, binary and hexadecimal number.	*6,K2,CO1*
		(ii) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bitword read out is as follows: (a) 000011101010 (b) 101110000110	*7,K2,CO1*
		OR	
	b)	Simplify the following four-variable Boolean function using K-Map F (A, B, C, D) = Σ (0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15) with logic gate implementation.	*13,K2,CO1*
12.	a)	Implement the following Boolean function with a 4 X 1 multiplexer and external gates. (i) F1 (A, B, C, D) = Σ (1, 3, 4, 11, 12, 13, 14, 15) (ii) F2 (A, B, C, D) = Σ (1, 2, 5, 7, 8, 10, 11, 13, 15)	*13,K3,CO2*

OR

b) Develop a 4-bit Binary to Gray Code and Gray to Binary Code Convertor. *13,K3,CO2*

13. a) Construct a JK flip-flop using a D Flip-flop and 2-to-1 line multiplexer. *13,K3,CO3*

OR

b) Design a four-bit binary synchronous counter with D flip-flops. *13,K3,CO3*

14. a) An Asynchronous circuit is described by the following excitation and output functions as. *13,K2,CO4*

$Y = x_1x_2' + (x_1 + x_2')\, y$

$Z = y$

Obtain the logic diagram, transition table, output map.

OR

b) Illustrate a PLA circuit to implement the following functions: *13,K2,CO4*

$F1 = A'B + AC + A'BC'$

$F2 = (AC + AB + BC)'$

15. a) Construct half adder and full adder using VHDL programming. *13,K3,CO5*

OR

b) Implement the any two counters using VHDL programming. *13,K3,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Summarize the features of Field Programmable Gate Array (FPGA) architecture with suitable diagram. *15,K2,CO4*

OR

b) Demonstrate the asynchronous sequential logic circuits transition table, flow table, race conditions, hazards and errors in digital circuits. *15,K2,CO4*