07 AUG 2023 AN

Reg. No.												

Question Paper Code	12122

B.E. / B.Tech - DEGREE EXAMINATIONS, APRIL / MAY 2023

Second Semester

Information Technology

(Common to Computer Science and Engineering, Computer Science and Engineering (IOT), Computer Science and Engineering (Cyber Security) & M.Tech. - Computer Science and Engineering)

20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Define Absorption Theorem.	*2,K1,CO1*
2.	Convert a given binary number 110111 into a decimal number system.	*2,K2,CO1*
3.	Illustrate the following Boolean function using 8:1 multiplexer $F(A,B,C)= \sum m(1,3,5,6)$.	*2,K2,CO2*
4.	Visualize the logic diagram of a one to four line demultiplexer.	*2,K1,CO2*
5.	Draw the state diagram of 3 bit Up/ Down Synchronous Counter.	*2,K2,CO3*
6.	Compare combinational circuits and sequential circuits.	*2,K2,CO3*
7.	Define a race condition.	*2,K1,CO4*
8.	Express a program for half adder using logic gates and write using Verilog HDL.	*2,K2,CO4*
9.	State the meaning of Hazards in sequential circuits.	*2,K1,CO5*
10.	Define State Assignment.	*2,K1,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Express the following Boolean expression in a simplified form using Boolean algebra. (i) X'Y'Z+X'YZ+XY' (ii) XYZ+X'Z+YZ.	*13,K2,CO1*
		OR		
	b)	Estimate the Minimal Sum of Products form of the Switching function $F(a,b,c,d)=\Sigma m(0,2,4,6,8)+\Sigma d(10,11,12,13,14,15)$.	*13,K2,CO1*
12.	a)	Illustrate a full subtractor and half subtractor and implement it by using basic gates. Write the design procedure.	*13,K3,CO2*

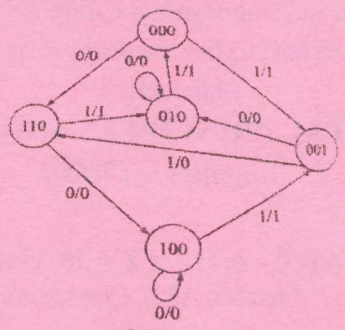
K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

OR

b) (i) Illustrate 4 x 16 decoder using two 3 x 8 decoders with enable input. *6,K2,CO2*

(ii) Find the following functions using a multiplexer. F(W,X,Y,Z)= ∑m (0,1,3,4,8,9,15). *7,K2,CO2*

13. a) Illustrate the design of a clocked sequential circuit using J-K flip-flop for the given state diagram. *13,K2,CO3*



OR

b) Implement the following :-

(i) T flip flop using SR flip –flop. *5,K2,CO3*

(ii) T flip-flop using D flip flop. *5, K2,CO3*

(iii) T flip-flop using JK flip flop. *3, K2,CO3*

14. a) (i) Demonstrate the characteristics of T flip-flop using the Verilog HDL. *7,K2,CO4*

(ii) Demonstrate the characteristics of S-R flip-flop using the Verilog HDL. *6,K2,CO4*

OR

b) (i) Interpret the working of universal shift registers. *7,K2,CO4*

(ii) Explain the working of a 3 bit asynchronous down counter. *6,K2,CO4*

15. a) Draw an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When the second input also becomes 1, z=0; the output stays at 0 until circuit goes back to initial state. *13,K2,CO5*

OR

b) Explain about hazards in digital systems with example. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) The following messages have been coded in the even parity hamming code and transmitted through a noisy Channel. Decode the messages, assuming that at most a single error has occurred in each code word.

(i) 1001001 *5,K2,CO6*

(ii) 0111001 *5,K2,CO6*

(iii) 1110110 *5,K2,CO6*

OR

b) Implement the following function using PAL.

F1 (A, B,C) = Σ(1, 2, 4, 6); *5,K2,CO6*

F2 (A, B, C) = Σ(0, 1, 6, 7); *5,K2,CO6*

F3 (A, B,C) = Σ(1, 2, 3, 5, 7). *5,K2,CO6*