

Reg. No.

Question Paper Code

21311

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV/ DEC 2023

First Semester

M.E. - Computer Science and Engineering (Specialization in Networks)

(Common to M.E. - Computer Science and Engineering)

20PCNPC101 - ADVANCED COMPUTER ARCHITECTURE

(Regulations 2020)

Duration: 3 Hours

Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

- | | <i>Marks,
K-Level, CO</i> |
|---|-------------------------------|
| 1. Write down the equation for calculating CPU performance Equation. | 2,K1,CO1 |
| 2. Define Data Hazards. | 2,K1,CO1 |
| 3. What do you mean by multiple Issue processor. | 2,K1,CO2 |
| 4. Define Principle of locality. | 2,K1,CO2 |
| 5. Differentiate Buses from crossbar networks. | 2,K2,CO3 |
| 6. Illustrate the Factors affecting the two components of miss rate in cache performance. | 2,K2,CO3 |
| 7. Differentiate between SMT and CMP. | 2,K2,CO4 |
| 8. Classify the elements of Interconnect Bus. | 2,K2,CO4 |
| 9. Compare scalar and vector processors. | 2,K2,CO5 |
| 10. Discuss SIMD. | 2,K1,CO5 |

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11. a) What is ILP? Discuss about the types of dependencies with example. 13,K2,CO1
- OR**
- b) Discuss how hardware based speculation is used to overcome control dependence. 13,K2,CO1
12. a) Explain the architecture and function of Super scalar processor. 13,K2,CO2
- OR**
- b) What is memory hierarchy? Elaborate the level in memory hierarchy with a diagram. 13,K2,CO2
13. a) Explain Centralized Shared Memory Architectures. 13,K2,CO3

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

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- b) Discuss in detail about the cache coherence protocols. 13,K2,CO3
14. a) (i) Describe the Computer Architecture of Warehouse-Scale Computers. 7,K2,CO4
 (ii) Explain the Physical Infrastructure and Costs of Warehouse-Scale Computers. 6,K2,CO4
- OR**
- b) (i) Suppose we have 8 memory banks with a bank busy time of 6 clocks and a total memory latency of 12 cycles. How long will it take to complete a 64-element vector load with a stride of 1? And with a stride of 32? Create the same. 7,K3,CO5
 (ii) Explain the Layer 3 network used to link arrays together and to the Internet. 6,K2,CO5
15. a) (i) Describe Vector Architecture in detail 7,K2,CO5
 (ii) Identify the need for SIMD Extension for multimedia. 6,K2,CO5
- OR**
- b) (i) Explain the details of handling Multidimensional Arrays in Vector Architectures. 7,K2,CO4
 (ii) Analyze how to Handle Sparse Matrices in Vector Architectures. 6,K2,CO4

PART - C (1 × 15 = 15 Marks)

16. a) Prepare the similarities and differences between the following 15,K3,CO6
 (i) Vector architectures and GPUs.
 (ii) Multimedia SIMD computers and GPUs.
- OR**
- b) Develop any four multicore architectures which you have studied, analyze the advantages and disadvantages and present a summary of it. 15,K3,CO6