Reg. No.												

Question Paper Code	21323

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

First Semester

M.E. - Embedded Systems Technologies

20PESPC101 - ADVANCED DIGITAL PRINCIPLES AND DESIGN

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level,CO
1.	List the basic building blocks in ASM chart.	*2,K1,CO1*
2.	Distinguish between Moore and Mealy FSM.	*2,K2,CO1*
3.	Define implication table.	*2,K1,CO2*
4.	Define hazard in sequential circuits.	*2,K1,CO2*
5.	Define stuck at 1 fault.	*2,K1,CO3*
6.	Define essential test vector.	*2,K1,CO3*
7.	Define slave mode.	*2,K1,CO6*
8.	What are the applications of FPGA.	*2,K1,CO6*
9.	Write a VHDL code for JK FLIP FLOP using Behavioural model.	*2,K2,CO4*
10.	Write a VHDL code for NAND gate using a data flow model.	*2,K2,CO4*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11. a) Design a sequence detector to detect the sequence 0111 using mealy and Moore FSM. *13,K2,CO1*

OR

b) Explain the design procedure for synchronous sequential circuits with an example. *13,K2,CO1*

12. a) Show the reduced state table for a given state table using a merger diagram and implication table. *13,K2,CO2*

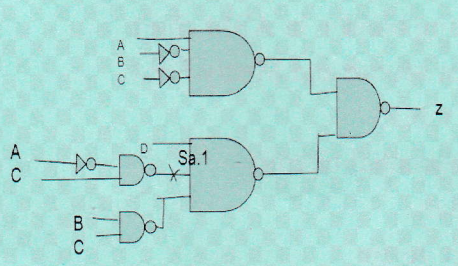
Present state	next state		output	
	x=0	x=1	x=0	x=1
a	d	b	0	0
b	e	a	0	0

c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

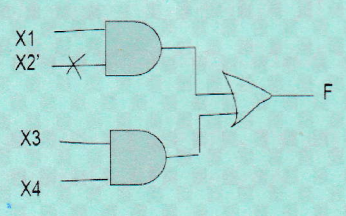
OR

b) What are hazards? List its types. Explain in detail about the static 1 hazard with an example *13,K2,CO2*

13. a) (i) For the below circuit, determine the test vector which detects the stuck at 1 fault using path sensitization method. *5,K2,CO3*



(ii) Analyze the given circuit using kohavi algorithm by a tests and b. test. *8,K2,CO3*



OR

b) Explain about fault diagnosis and testing process. *13,K2,CO3*

14. a) Explain the design flow of FPGA. *13,K2,CO6*

OR

b) Explain the input, output blocks and programmable interconnects of Xilinx 4000 family. *13,K2,CO6*

15. a) Write a VHDL code for ring counter. *13,K2,CO4*

OR

b) Write a VHDL code for half adder and full adder using a data flow model. *13,K2,CO4*

PART - C (1 × 15 = 15 Marks)

16. a) Implement full adder and full subtractor using PAL *15,K2,CO5*

OR

b) Implement BCD to excess 3 code convertor using PAL *15,K2,CO5*