Reg. No.												

Question Paper Code	11506

B.E./B.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

Sixth Semester

Electronics and Communication Engineering

EC8095 - VLSI DESIGN

(Regulations 2017)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level,CO
1.	Give the various color coding used in stick diagram.	2,K1,CO1
2.	Describe the channel length modulation and its effects in nMOS transistor.	2,K1,CO1
3.	Draw a 2-input XOR using pass transistor using nMOS pass transistor logic.	2,K2,CO2
4.	Define Pipelining.	2,K1,CO2
5.	Write the full adder output in terms of propagate and generate.	2,K1,CO4
6.	Why is barrel shifter very useful in the designing of arithmetic circuits?	2,K2,CO4
7.	List out the advantages and limitations of 3T DRAM over 1T DRAM.	2,K1,CO5
8.	State the three important blocks in FPGA Architecture.	2,K1,CO5
9.	What is the need for testing?	2,K1,CO6
10.	List the common techniques for ad hoc testing.	2,K1,CO6

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Express about the CV characteristics of MOS transistor along with neat sketches.	13,K2,CO1
		OR	
	b)	Explain in detail of the DC transfer characteristics of CMOS inverter.	13,K2,CO1
12.	a)	(i) Design a CMOS logic circuit for the given expression Z=(A(B+C)+DE)'.	6,K3,CO2
		(ii) List out the limitations of pass transistor logic. Explain any two techniques used to overcome the drawback of pass transistor logic.	7,K2,CO2
		OR	
	b)	Implement C^2MOS logic and explain how 0-0 and 1-1 overlap of clock signals are eliminated.	13,K2,CO2
13.	a)	Describe the working of ripple carry adder and derive the expression for worst case delay.	13,K2,CO4

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

OR

b) Construct 4×4 array type multiplier and find its critical path delay. *13,K3,CO4*

14. a) Describe FPGA interconnect routing resources with neat diagram. *13,K2,CO5*

OR

b) Draw and explain the architecture of large memory array with sub array memory circuitry. *13,K2,CO5*

15. a) Describe briefly about the BIST block structure along its components. *13,K2,CO6*

OR

b) Discuss in detail about different types of scan design method and explain with neat diagram. *13,K2,CO6*

PART - C (1 × 15 = 15 Marks)

16. a) Classify the sources of power dissipation and derive the equation for each parameter. *15,K3,CO3*

OR

b) Discuss the different timing parameters that characterize the timing of sequential circuit. *15,K2,CO3*