Reg. No.													

Question Paper Code	11576

B.E./B.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

Fifth Semester

Electronics and Communication Engineering

20ECPC502 - VLSI DESIGN

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

PART-A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Name the different operating modes of transistor and its current equation.	*2,K1, CO1*
2.	Define body effect and write the threshold equation including the body effect.	*2,K1, CO1*
3.	Define Ganged CMOS.	*2,K1, CO2*
4.	Trace the recharge and evaluation modes of dynamic gates timing diagram.	*2,K2, CO3*
5.	Define Pipelining.	*2,K1, CO2*
6.	Define Max –delay failure and Min- delay failure in sequential circuits.	*2,K1, CO3*
7.	List some of the identifiers used in Verilog.	*2,K1, CO4*
8.	Classify the timing control.	*2,K2, CO4*
9.	List the use of Booth Encoder.	*2,K1, CO5*
10.	Examine the applications of CAM.	*2,K1, CO6*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Illustrate about the Non ideal I-V effects of MOS transistors with neat diagram.	*13,K2,CO1*
		OR	
	b)	(i) Identify the relationship between V_{gs} versus V_{ds} versus I_{ds}.	*8,K2,CO1*
		(ii) Explain N-Well layout design rules.	*5,K2,CO1*
12.	a)	Explain in detail about static CMOS logic (or) complementary CMOS logic.	*13,K2,CO2*
		OR	
	b)	(i) Discuss in detail about the Skewed Gates.	*7,K2,CO2*
		(ii) Explain in detail about the CVSL gates.	*6,K2,CO2*

13. a) Discuss in detail about choosing a clocking strategy. *13,K2,CO3*

OR

b) Explain the timing issues related to sequential logic circuits. *13,K2,CO3*

14. a) Write a Verilog program to simulate a 4 bit ripple carry adder by instantiating four full adders. *13,K3,CO4*

OR

b) Illustrate System tasks and Compiler Directives with examples. *13,K2,CO4*

15. a) Explain the power and speed trade-offs with suitable case study. *13,K2,CO5*

OR

b) Explain the operation of Carry Bypass adder with neat diagram. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Explain the architecture of large memory array with sub array memory circuitry. *15,K2,CO6*

OR

b) Describe the working of Multi-ported SRAM and Register file CMOS logic circuit. *15,K2,CO6*