06 FEB 2023

COE

Reg. No.												

Question Paper Code	11682

B.E./B.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2022

Third Semester

Electronics and Communication Engineering

20ECPC301 - DIGITAL ELECTRONICS

(Regulations 2020)

Duration: 3 Hours

Max. Marks: 100

PART-A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	State De Morgan's theorem and mention its use.	2,K1,CO1
2.	Convert binary 110111 into a decimal number system.	2,K2,CO1
3.	Draw the full adder circuit using half adder.	2,K1,CO2
4.	Explain Combinational logic circuit?	2,K2,CO2
5.	Explain how can race around conditions be eliminated?	2,K2,CO3
6.	Differentiate between the edge triggering and level triggering.	2,K2,CO3
7.	State the rules for state reduction.	2,K1,CO4
8.	Differentiate synchronous and asynchronous sequential circuits.	2,K2,CO4
9.	Define noise margin.	2,K1,CO6
10.	Define power dissipation and propagation delay.	2,K1,CO6

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Use Quine Mccluskey method to simplify the given expression and verify your result using K-map F(A,B,C,D)=∑(0,2,3,5,7,9,11,13,14).	13,K3,CO1
		OR	
	b)	Determine the minimum SOP expression F(A,B,C,D,E)=m(1,4,6,10,20,22,24,26)+d(0,11,16,27) using K-map method. Draw the circuit of the minimal expression using only NAND gates.	13,K3,CO1
12.	a)	With a neat diagram, explain in detail about the working of a 4 –bit look ahead carry adder. Also mention its advantage over conventional adder.	13,K3,CO2
		OR	
	b)	Construct a 4-bit comparator using logic gates.	13,K2,CO2

13. a) Draw and explain the 4-bit SISO, SIPO, PISO and PIPO shift register with its waveforms. 13,K2,CO3

OR

b) (i) Explain the operation of JK flip flop with neat diagram. 7,K2,CO3
(ii) Convert to D flip-flop from a J-K flip-flop. 6,K2,CO3

14. a) Construct a MOD-10 synchronous counter using JK flip flops. Write an execution table and state table. 13,K3,CO4

OR

b) Explain dynamic and essential hazard with an example. 13,K2,CO4

15. a) Construct the following four Boolean functions using PAL. 13,K3,CO6
F1(W,X,Y,Z) =∑m(0,1,2,3,7,9,11)
F2(W,X,Y,Z) =∑m(0,1,2,3,10,12,14)
F3(W,X,Y,Z) =∑m(0,1,2,3,10,13,15)
F4(W,X,Y,Z) =∑m(4,5,6,7,9,15)

OR

b) Explain the operation of TTL with neat diagram. 13,K2,CO6

PART C (1 × 15 = 15 Marks)

16. a) An asynchronous sequential circuit is described by the excitation and output functions. 15,K3,CO5
Y= x1x2' + (x1 + X2')y
Z=Y
(i) Draw the logic diagram of the circuit.
(ii) Give the transition table and output map.
(iii) Give the state flow table.

OR

b) Construct an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input is transferred to Z. When Y is 0, the output does not change for any change in X. 15,K3,CO5