24-04-2023

Reg. No.												

Question Paper Code	11801

B.E. / B.Tech. - DEGREE EXAMINATIONS, APR/MAY 2023

Seventh Semester

Electronics and Communication Engineering

EC8095 - VLSI DESIGN

(Regulations 2017)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level,CO
1.	List the merits and demerits of scaling.	*2,K1,CO1*
2.	Name the different operating modes of transistor and its Current equation.	*2,K1,CO1*
3.	Trace the recharge and evaluation modes of dynamic gates timing diagram.	*2,K2,CO2*
4.	Define Logic restructuring.	*2,K1,CO2*
5.	Discuss about local-skew and global skew.	*2,K1,CO3*
6.	Express the dynamic dissipation equation of CMOS inverter.	*2,K2,CO3*
7.	State bit sliced data path organization.	*2,K1,CO4*
8.	Why is barrel shifter very useful in the designing of arithmetic circuits?	*2,K2,CO4*
9.	Name the elements in configurable logic block	*2,K1,CO5*
10.	Compare serial and parallel scan in adhoc testing.	*2,K2,CO6*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Illustrate about the Non ideal I-V effects of MOS transistors With neat diagram.	*13,K2,CO1*
		OR	
	b)	Summarize the MOS model with necessary equations. (i) Simple MOS capacitance model. (ii) Detailed MOS gate capacitance and diffusion capacitance model	*6,K2,CO1* *7,K2,CO1*
12.	a)	Express the CVSL logic for inverter, NAND and 4 Input XOR gate.	*13,K2,CO2*
		OR	
	b)	(i) Represent the static CMOS circuit for the following expressions. 1. F=(A[B+C])+DE)' 2. F=(A+B+CD)' (ii) Illustrate Pseudo-nMOS circuits in detail.	*8,K2,CO2* *5,K2,CO2*

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

13. a) Classify the types of power dissipation and derive the equation for each parameter. *13,K2,CO3*

OR

b) Explain the timing issues related sequential logic circuits. *13,K2,CO3*

14. a) Describe the working of ripple carry adder and derive the expression for worst case delay. *13,K2,CO4*

OR

b) Illustrate the working of 4x4 carry save multiplier with neat diagram. Summarize the number of adders. Compare it over the Wallace Tree multiplier. *13,K2,CO4*

15. a) With neat Sketch explain the CLB, IOB and programmable interconnects of an FPGA device. *13,K2,CO5*

OR

b) Explain routing procedures involved in FPGA interconnect. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Draw the block diagram of BILBO\BIST and explain each unit operation. *15,K2,CO6*

OR

b) Examine the boundary scan architectures and explain how to test the circuit board level and system level. *15,K2,CO6*