Reg. No.												

Question Paper Code	11834

B.E./B.Tech. - DEGREE EXAMINATIONS, APRIL/MAY 2023

Seventh Semester

Electronics and Communication Engineering

EC8791 – EMBEDDED AND REAL TIME SYSTEMS

(Regulations 2017)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Outline the challenges in embedded computing system design.	*2,K2,CO2*
2.	Define Quality Assurance Techniques.	*2,K1,CO2*
3.	Illustrate the three different profiles of ARM cortex Processor.	*2,K2,CO1*
4.	Find the differences between MULS and MULSEQ.	*2,K1,CO1*
5.	Outline the significance of CDFG.	*2,K2,CO3*
6.	Show the limitation of RM algorithm.	*2,K1,CO4*
7.	Compare the difference between release time and deadline.	*2,K2,CO4*
8.	List the factors on which the program runtime estimation depends.	*2,K1,CO5*
9.	What are fault containment zones and error containment ones?	*2,K1,CO5*
10.	Differentiate between shared memory and message passing in multiprocessors concept.	*2,K2,CO6*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Analyze the hierarchical design flow for an embedded system with suitable diagrams.	*13,K2,CO2*
		OR	
	b)	Elaborate the following as per system level design analysis; (i) Consumer electronics architecture. (ii) Quality Assurance techniques. (iii) Architecture design.	*4,K2,CO2* *5,K2,CO2* *4,K2,CO2*
12.	a)	Discuss about the types of stacks and subroutines supported by ARM processor.	*13,K2,CO1*
		OR	
	b)	(i) Estimate the value to be given in PWMMR0 and PWMMR3 to get a pulse train of period 5 ms and duty cycle of 25%.	*7,K2,CO1*
		(ii) Evaluate the features of LPC 214x processor.	*6,K2,CO1*

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

13. a) For the given conditional code snippet, develop the code *13,K3,CO3*

```
if (a + b > 0)
    x = 5;
else
    x = 7;
```

OR

b) Discuss with necessary diagrams, the program level performance analysis. Frame the key features of clear box testing. *13,K2,CO3*

14. a) Examine the exponentially distributed fault latency with the condition mean is equal to $1/\mu$. *13,K3,CO4*

OR

b) Interpret the uniprocessor scheduling algorithms in developing a multiprocessor schedule. *13,K2,CO4*

15. a) (i) Explain utilization balancing task assignment algorithm in detail. *6,K2,CO5*

(ii) Explain fault containment and error containment in fault tolerant real time systems in detail. *7,K3,CO5*

OR

b) Explain EDF in detail. Schedule the following process using EDF. *13,K3,CO5*

Process	Execution Time	Period
P1	1	3
P2	1	4
P3	2	5

PART - C (1 × 15 = 15 Marks)

16. a) (i) Justify this statement with the help of an example. The timing requirements on a set of processes can strongly influence the type of appropriate scheduling. *10,K2,CO6*

(ii) Write about a critical section using semaphores in the operating system. *5,K3,CO6*

OR

b) Design a simple engine control unit (ECU) which controls the operation of a fuel- injected engine based on several measurements taken from the running engine. *15,K3,CO6*