Reg. No.												

Question Paper Code	11926

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL/MAY 2023

Fifth Semester

Electronics and Communication Engineering

20ECPC502 - VLSI DESIGN

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level,CO
1.	Name the different operating modes of transistor and its current equation.	2,K1,CO1
2.	Define body effect and write the threshold equation including the body effect.	2,K1,CO1
3.	List the advantages of static CMOS design.	2,K1,CO2
4.	Define Ganged CMOS.	2,K1,CO2
5.	Define Setup time and Hold time.	2,K1,CO3
6.	Define Clock Skew and Clock jitter.	2,K1,CO3
7.	List the value sets in Verilog.	2,K1,CO4
8.	Explain the functions of $monitor, $display and $strobe.	2,K2,CO4
9.	List the use of Booth Encoder.	2,K1,CO5
10.	State bit sliced data path organization.	2,K1,CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Explain the delay models with suitable diagrams.	13,K2,CO1
		OR	
	b)	Illustrate about the Non ideal I-V effects of MOS transistors with neat diagram.	13,K2,CO1
12.	a)	Explain the ratioed logic with suitable diagram.	13,K2,CO2
		OR	
	b)	(i) Represent the static CMOS circuit for the following expressions. (a) F =(A[B+C])+DE)' (b) F=(A+B+CD)'	7,K2,CO2
		(ii) Trace the supporting diagrams and write short notes on Bubble pushing.	6,K2,CO2

13. a) Discuss the following power dissipation techniques and its impact in CMOS inverter circuits.
(i) Static dissipation — *7,K2,CO3*
(ii) Dynamic dissipation. — *6,K2,CO3*

OR

b) Explain in detail about the pipeline concepts used in sequential circuits Sequencing Methods. — *13,K2,CO3*

14. a) Construct a Verilog program for 3:8 decoder using any modeling. — *13,K3,CO4*

OR

b) Illustrate System tasks and Compiler Directives with examples. — *13,K2,CO4*

15. a) Illustrate the working of 4x4 carry save multiplier with neat diagram. Summarize the number of adders. Compare it over the Wallace Tree multiplier. — *13,K2,CO5*

OR

b) Describe the working of ripple carry adder and derive the expression for worst case delay. — *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Explain the architecture of large memory array with sub array memory circuitry. — *15,K2,CO6*

OR

b) Explain about the DRAM sub array and open bit lines architecture. — *15,K2,CO6*