| Reg. No. | | | | | | | | | | | | | |
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| Question Paper Code | 12023 |
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18 JUL 2023

**B.E./B.Tech - DEGREE EXAMINATIONS, APRIL / MAY 2023**

Third Semester

**Electronics and Communication Engineering**

**20ECPC301 - DIGITAL ELECTRONICS**

(Regulations 2020)

Duration: 3 Hours | Max. Marks: 100

**PART - A (10 × 2 = 20 Marks)**

Answer ALL Questions

| | | Marks, K-Level, CO |
|---|---|---|
| 1. | Prove the following using De Morgan's Theorem, $[(x+y)' + (x+y)']' = x+y$. | 2,K1,CO1 |
| 2. | Interpret the function Y = A + B'C in canonical POS. | 2,K2,CO1 |
| 3. | Implement Full adder using two half adders. | 2,K2,CO2 |
| 4. | Differentiate a decoder from a demultiplexer. | 2,K2,CO2 |
| 5. | Realize T Flip Flop using SR Flip Flop. | 2,K2,CO3 |
| 6. | The content of a 4-bit register is initially 1101. The register is shifted 6 times to the right with the serial input being 101101. What is the content of the register after each shift? | 2,K2,CO3 |
| 7. | What is called dynamic hazard in asynchronous sequential circuit? | 2,K1,CO4 |
| 8. | Distinguish between non-critical race and critical race. | 2,K2,CO4 |
| 9. | Why totem pole outputs cannot be connected together? | 2,K2,CO5 |
| 10. | A certain memory has a capacity of 32K x 16. How many bits are there in each word? How many words are being stored and how many memory cells does this memory contain? | 2,K2,CO5 |

**PART - B (5 × 13 = 65 Marks)**

Answer ALL Questions

| | | | |
|---|---|---|---|
| 11. | a) | Simplify the following Boolean expression using K map and draw the logic diagram. $F=\sum m(1,4,8,10,11,20,22,24,25,26)+d(0,12,16,17)$ | 13,K2,CO1 |
| | | **OR** | |
| | b) | Implement the following function using Quine McCluskey method. $F = \sum m(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$. | 13,K2,CO1 |
| 12. | a) | Design a 4-bit BCD adder using full adder and explain its structure and compute the circuit to add 1001 and 0101. Write the sum and carry output of the given binary number. | 13,K3,CO2 |

**OR**

b) Design 3-bit magnitude comparator using logic gates. *13,K3,CO2*

13. a) Design a synchronous 3-bit counter which counts in the sequence 1, 3, 2,6, 7, 5, 4,(repeat) 1,3..... using T FF. *13,K3,CO3*

**OR**

b) A sequential circuit has two JK flip-flops A and B, two inputs $x$ and $y$ and one output $z$. The flip-flop input equations and circuit output equation are: *13,K3,CO3*

$J_A = Bx + B'y' J_B = A'x$

$K_A = B'xy' K_B = A + xy'z = Axy + Bx'y'$

Draw the logic diagram and state table of the circuit. Also derive the state equations for A and B.

14. a) An asynchronous sequential circuit is described by the following excitation and output function.

$Y = X_1X_2' + (X_1 + X_2')Y, Z = Y$

(i) Draw the logic diagram. *5,K3,CO4*

(ii) Derive the transition table and output map. *4,K3,CO4*

(iii) Describe the behaviour of the circuit. *4,K3,CO4*

**OR**

b) What is the objective of state assignment in an asynchronous circuit? Give the hazard free realization for the Boolean function $f(A, B, C, D) = M(0, 2, 6, 7, 8, 10, 12)$. *13,K3,CO4*

15. a) Design and implement a BCD to Gray code converter using PLA. *13,K3,CO5*

**OR**

b) Select a 4096 x 8 bit ROM memory to store the driver program of the Robotic design. The memory chip of has two chips select inputs and operates from a 5v power supply. How many pins are needed for the integrated circuit package? Draw a block diagram and label all input and output terminals in the ROM. *13,K3,CO5*

**PART - C (1 × 15 = 15 Marks)**

16. a) Design an even parity generator that generates an even parity bit for every input string of 3-bits. *15,K3,CO6*

**OR**

b) Explain the operation of TTL with neat diagram. *15,K2,CO6*