Reg. No.												

Question Paper Code	12066

21 JUL 2023

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2023

Fourth Semester

Electronics and Communication Engineering

20ECPW401 - ELECTRONIC CIRCUITS WITH LABORATORY

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Explain the need for biasing.	*2,K2,CO1*
2.	Explain why we choose Q point at the center of the load line.	*2,K1,CO1*
3.	Two identical amplifiers having 10dB gain each are cascaded. Calculate the output, if the input is of 1mV (P-P).	*2,K2,CO2*
4.	Draw the h parameter equivalent model of a CB BJT amplifier.	*2,K2,CO2*
5.	A tuned amplifier has its maximum gain at a frequency of 2 MHz and has a bandwidth of 50 KHz. Calculate the Q factor.	*2,K2,CO4*
6.	Draw the ideal response and actual response of tuned amplifiers with a diagram.	*2,K2,CO4*
7.	Compare Astable, Monostable and Bistable multivibrators.	*2,K2,CO5*
8.	List out the reason for Schmitt trigger acting as a zero crossing detector.	*2,K1,CO5*
9.	List the characteristics of Class B amplifiers.	*2,K1,CO6*
10.	Define power amplifier.	*2,K1,CO6*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	(i) Express the stability factor S, S' and S'' of emitter bias circuit.	*8,K2,CO1*
		(ii) Design a fixed biased circuit using silicon transistor having $\beta = 120, V_{CC} = 12V, V_{CE} = 5V$ and $I_C = 5mA$.	*5,K3,CO1*
		OR	
	b)	Construct a voltage divider bias circuit and derive its stability factor and also give reasons why it is advantageous than fixed bias circuit.	*13,K2,CO1*
12.	a)	Derive the expression for the voltage gain of Common Drain (Source Follower) FET Amplifier.	*13,K2,CO2*
		OR	
	b)	Using a low frequency h-parameter model, derive the expressions for voltage gain, current gain, input impedance and output admittance of a BJT Amplifier in CE configuration.	*13,K2,CO2*

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

13. a) Draw the circuit diagram and equivalent circuit of a capacitor coupled single tuned amplifier and derive the expression for 3 – dB bandwidth, sketch the frequency response for the same. *13,K2,CO4*

OR

b) With a neat circuit diagram derive the expression for 3dB bandwidth of a double tuned amplifier. *13,K2,CO4*

14. a) Explain the working principle of Astable multivibrator with neat diagrams and also derive the expression for time period T. *13,K2,CO5*

OR

b) Illustrate why Neutralization is needed in tuned amplifier and explain Hazeltine and Neutrodyne neutralization techniques with neat circuit diagram. *13,K2,CO5*

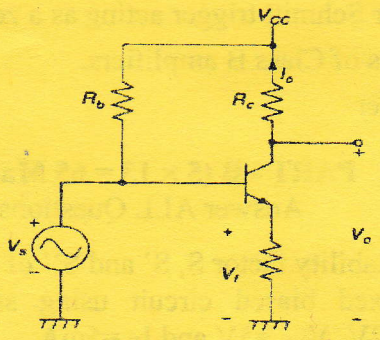
15. a) Explain the working of Class-B Push-Pull power amplifiers employing input and output transformers with the help of a neat circuit diagram. Discuss its advantages and disadvantages. *13,K2,CO6*

OR

b) Draw the circuit diagram of Class-AB complementary / symmetry power amplifier with its load line and explain its operation. Give the expression for dc power input, ac power output and efficiency. *13,K2,CO6*

PART - C (1 × 15 = 15 Marks)

16. a) For the given below circuit diagram determine the type of feedback topology and also derive the input and output impedance. *15,K3,CO3*



OR

b) Discuss the effects of negative feedback on stability, distortion, noise, Bandwidth, input and output impedance of a feedback amplifier. *15,K2,CO3*