Reg. No.															

Question Paper Code	13311

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Third Semester

Computer Science and Business Systems

20CBPC302 - COMPUTER ORGANIZATION AND ARCHITECTURE

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (20 × 1 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The interconnection between arithmetic logic unit and the register is called (a) process route (b) information trail (c) information path (d) data path	1	K1	CO1
2.	Which of the following register is used in the control unit of the CPU to indicate the next instruction which is to be executed? (a) Program counter (b) Instruction decoder (c) Index register (d) Accumulator	1	K1	CO1
3.	The length of a register is called (a) register limit (b) register size (c) word size (d) word limit	1	K1	CO1
4.	What is the primary difference between RISC and CISC ISAs? (a) CISC uses fixed-length instructions (b) RISC instructions are typically longer (c) CISC has a smaller set of instructions (d) RISC uses more complex instruction formats	1	K1	CO2
5.	The decoded instruction is stored in (a) memory data register (MDR) (b) register (c) program counter (PC) (d) instruction register (IR)	1	K1	CO2
6.	What does ISA stand for in computer organization and architecture? (a) Integrated software application (b) Internal system architecture (c) Instruction set algorithm (d) Instruction set architecture	1	K1	CO2
7.	When rounding a floating-point number to a lower precision, which digits are discarded? (a) Leading digits (b) Trailing digits (c) Integer part (d) Exponent	1	K1	CO3
8.	When performing floating-point addition, which step typically involves aligning the exponents of the two operands? (a) Normalization (b) Exponentiation (c) Fractionation (d) Precision adjustment	1	K1	CO3
9.	In floating-point arithmetic, what does the term "mantissa" represent? (a) The exponent (b) The sign bit (c) The fractional part (d) The integer par	1	K1	CO3
10.	A hardwired control unit uses logic to generate control signals based on the current instruction being executed. (a) microcode (b) combinational (c) sequential (d) assembly language	1	K1	CO4
11.	What is the primary purpose of the x86 EFLAGS register? (a) Handling floating-point arithmetic (b) Controlling program flow (c) Managing memory addresses (d) Storing the result of arithmetic operations	1	K1	CO4
12.	What is the Pipeline stall called? (a) Load use pipeline stall (b) Bubble (c) Load use data stall (d) Data stall	1	K1	CO4
13.	What does DMA stand for in computer architecture? (a) Direct Memory Access (b) Dynamic Memory Access (c) Direct Machine Access (d) Data Management Access	1	K1	CO5
14.	Which transfer mechanism interrupts the CPU only when data is available? (a) Program Controlled (b) Interrupt Driven (c) DMA (d) Polled	1	K1	CO5
15.	Which of the following is an example of an input device? (a) Printer (b) Monitor (c) Keyboard (d) Speaker	1	K1	CO5

16. What does USB stand for? *1 K1 CO5*
    (a) Universal Serial Bus (b) Unified Serial Bus
    (c) Universal Signal Bus (d) Unified Signal Bus
17. In memory interleaving, the memory addresses are divided into: *1 K1 CO6*
    (a) Multiple banks (b) Multiple caches (c) Multiple registers (d) Multiple processors
18. What is the trade-off between cache size and block size? *1 K1 CO6*
    (a) Larger block size decreases hit rate
    (b) Larger block size increases cache misses
    (c) Larger cache size increases hit rate but also cost
    (d) Larger cache size decreases power consumption
19. Which replacement algorithm replaces the least recently used block in cache? *1 K1 CO6*
    (a) Random replacement (b) First-in-first-out (FIFO)
    (c) Least recently used (LRU) (d) Least frequently used (LFU)
20. The process of replacing an existing block in cache with a new one is called---------- *1 K1 CO6*
    (a) Cache allocation (b) Cache replacement (c) Cache mapping (d) Cache shifting

PART - B (10 × 2 = 20 Marks)

Answer ALL Questions

21. What is Addressing mode? *2 K1 CO1*
22. Define Boolean Logic. *2 K1 CO1*
23. List the names of the registers. *2 K1 CO2*
24. Define instruction set Architecture. *2 K1 CO2*
25. What is the principle of booth multiplication? *2 K1 CO3*
26. List out the major categories of parallel multiplier implementation. *2 K1 CO3*
27. What is Cache Coherence? *2 K1 CO4*
28. What is meant by hardwired control? *2 K1 CO4*
29. Define PROMs. *2 K1 CO5*
30. Compare cache size and block size. *2 K2 CO6*

PART - C (6 × 10 = 60 Marks)

Answer ALL Questions

31. a) Explain the Instruction Execution Cycle, detailing each step involved in executing an instruction. *10 K2 CO1*

    OR

    b) Illustrate various Addressing Modes with relevant examples to each mode. *10 K2 CO1*

32. a) Summarize the process of instruction interpretation in a computer system. What factors influence how instructions are executed? *10 K2 CO2*

    OR

    b) Compare and contrast Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC) architectures. *10 K2 CO2*

33. a) Explain Fixed and Floating Point representation with suitable examples. *10 K2 CO3*

    OR

    b) Explain the principle of Shift and Add Multiplication with suitable examples. *10 K2 CO3*

34.	a)	Explain Flynn's classification of computer architectures.	*10*	*K2*	*CO4*
		OR			
	b)	Show a flowchart that outlines the instruction fetch-decode-execute cycle in a pipelined CPU.	*10*	*K2*	*CO4*
35.	a)	Illustrate Peripheral devices with examples.	*10*	*K2*	*CO5*
		OR			
	b)	Explain the key characteristics of SCSI (Small Computer System Interface) and give the advantages and disadvantages.	*10*	*K2*	*CO5*
36.	a)	Explain in detail about Cache memory and its principles.	*10*	*K2*	*CO6*
		OR			
	b)	Explain the concept of hierarchical memory organization.	*10*	*K2*	*CO6*