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| Question Paper Code | 12552 |
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**B.E. / B.Tech - DEGREE EXAMINATIONS, NOV / DEC 2023**  
Third Semester  
**Computer and Communication Engineering**  
**20CCPC301 - DIGITAL LOGICS AND SYSTEM DESIGN**  
(Regulations 2020)

Duration: 3 Hours

Max. Marks: 100

**PART - A (10 × 2 = 20 Marks)**  
Answer ALL Questions

- |  | <i>Marks,</i><br><i>K-Level, CO</i> |
|--|-------------------------------------|
| 1. State the Features of ECL.  | 2,K1,CO1                            |
| 2. Infer how conversion of 0.6875, decimal value to Octal & Binary occurs?                       | 2,K2,CO1                            |
| 3. State the difference between Demux and Decoder.   | 2,K1,CO2                            |
| 4. Infer the following Boolean function using 8:1 multiplexer<br>$F(A,B,C)=\sum(1,3,5,6)$ .      | 2,K2,CO2                            |
| 5. Define Flow Table.  | 2,K1,CO4                            |
| 6. Identify, what is the minimum number of Flip Flops required to design a counter of modulo 60? | 2,K2,CO4                            |
| 7. Distinguish between Critical and Non critical Races.  | 2,K2,CO5                            |
| 8. Outline the steps for the design of asynchronous sequential circuit.                          | 2,K2,CO5                            |
| 9. What is memory decoding?  | 2,K1,CO6                            |
| 10. Distinguish between PAL, PLA and PROM.   | 2,K2,CO6                            |

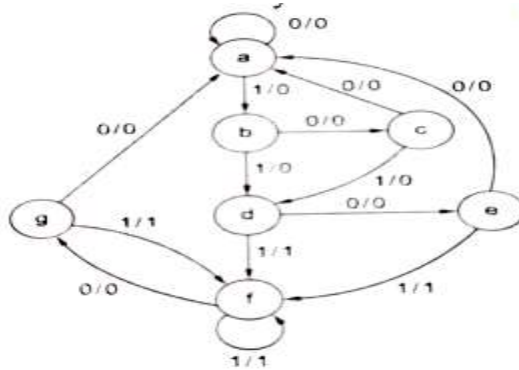
**PART - B (5 × 13 = 65 Marks)**  
Answer ALL Questions

11. a) Explain the working principle of Hamming Code with an example. State its advantages over parity codes. 13,K2,CO1
- OR**
- b) Write short notes on 13,K1,CO1
- (i) RTL
- (ii) ECL
12. a) Implement a staircase light, which is controlled by two-way switches, one is at the top of the stairs and the other is at the bottom of the stairs.
- (i) Make a truth table for this system. 3,K3,CO2
- (ii) Write the logic function in SOP form. 3,K3,CO2
- (iii) Realize the circuit using basic logic gates. 3,K3,CO2
- (iv) Realize the circuit using minimum number of NAND and NOR gates. 4,K3,CO2

**OR**

b) Construct the BCD code to Excess 3 code with neat logical diagram. 13,K3,CO2

13. a) Outline a sequential circuit for a given state diagram, use state reduction if necessary and also use D - flip-flop and give what is the aim of Set reduction? 13,K2,CO4



**OR**

b) Explain the universal shift registers with neat diagram. 13,K2,CO4

14. a) (i) What is a Hazard? Give hazard free realization for the following Boolean function.  $F(A, B, C, D) = \sum m(1,5,6,7)$  using AND- OR gate network. 9,K2,CO5

(ii) Define Essential Hazards with an example. 4,K1,CO5

**OR**

b) Illustrate the design an asynchronous sequential circuit with inputs  $x_1$  and  $x_2$  and one output  $z$ . Initially and at any time if both the inputs are 0, output is equal to 0. When  $x_1$  or  $x_2$  becomes 1,  $z$  becomes 1. When second input also becomes 1,  $z=0$ ; the output stays at 0 until circuit goes back to initial state. 13,K2,CO5

15. a) Explain how a BCD to Excess-3 code converter designed and implement the same using suitable PLA. 13,K2,CO6

**OR**

b) (i) Illustrate the following Boolean functions using  $8 \times 2$  PROM.  $F_1 = \sum m(3,5,6,7)$  and  $F_2 = \sum m(1,2,3,4)$ . 6,K2,CO6

(ii) Implement the following Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs.  $F_1 = \sum m(3,5,6,7)$  and  $F_2 = \sum m(1,2,3,4)$ . 7,K2,CO6

**PART - C (1 × 15 = 15 Marks)**

16. a) Develop a verilog program for Full Subtractor and explain its timing diagram waveform. 15,K3,CO3

**OR**

b) Design a verilog HDL code for  $4 \times 1$  MUX and  $1 \times 4$  DEMUX. 15,K3,CO3