| Reg. No. | | | | | | | | | | | | |
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| Question Paper Code | 12899 |
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**B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024**

Third Semester

**Computer and Communication Engineering**

**20CCPC301 - DIGITAL LOGICS AND SYSTEM DESIGN**

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

**PART - A (10 × 2 = 20 Marks)**

Answer ALL Questions

| | | Marks | K – Level | CO |
|---|---|---|---|---|
| 1. | Infer how to convert a given binary number 110111 into a decimal number system? | 2 | K2 | CO1 |
| 2. | What is Fan in and Fan out of a gate? | 2 | K1 | CO1 |
| 3. | List the data types of Verilog. | 2 | K1 | CO3 |
| 4. | Illustrate the Verilog code for the AND gate. | 2 | K2 | CO3 |
| 5. | State the differences between combinational and sequential circuits. | 2 | K1 | CO4 |
| 6. | What is race around condition in flip flop? | 2 | K1 | CO4 |
| 7. | Distinguish between fundamental and pulse mode asynchronous sequential circuits. | 2 | K2 | CO5 |
| 8. | Outline critical race. | 2 | K2 | CO5 |
| 9. | Write short notes on PLA. | 2 | K1 | CO6 |
| 10. | What is a volatile memory? | 2 | K1 | CO6 |

**PART - B (5 × 13 = 65 Marks)**

Answer ALL Questions

| | | | Marks | K – Level | CO |
|---|---|---|---|---|---|
| 11. | a) | Explain in detail the parity generator and checker circuits with an example data. | 13 | K2 | CO1 |
| | | **OR** | | | |
| | b) i) | Interpret the conversion of $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent. | 6 | K2 | CO1 |
| | ii) | State the operation of RTL with a neat diagram. | 7 | K1 | CO1 |
| 12. | a) | Demonstrate with Verilog codes for the design of all basic and universal gates. | 13 | K3 | CO3 |
| | | **OR** | | | |
| | b) | Implement a Verilog code for Half adder and Full adder using Gate/Data Level Modelling. | 13 | K3 | CO3 |

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|---|---|---|---|---|---|
| 13. | a) | Illustrate the design procedure of a MOD-5 synchronous counter using JK flip-flops and implement it. | *13* | *K2* | *CO4* |
| | | **OR** | | | |
| | b) | Define Shift Register and explain the operation of 4-bit SIPO and PIPO shift register and draw its waveforms. | *13* | *K2* | *CO4* |
| 14. | a) | An asynchronous sequential circuit is described by the following excitation and output function. $Y= X_1X_2+(X_1+X_2)\ Y$, $Z=Y$.<br>i) Draw the logic diagram.<br>ii) Derive the transition table and output map.<br>iii) Illustrate the behavior of the circuit | *13* | *K2* | *CO5* |
| | | **OR** | | | |
| | b) | Illustrate about different hazards that occur in sequential circuits and also about the way to eliminate them. | *13* | *K2* | *CO5* |
| 15. | a) | Explain about the FPGA and CPLD. | *13* | *K2* | *CO5* |
| | | **OR** | | | |
| | b) i) | Illustrate the Gray to Binary code converter and derive the circuitry used to realize them using PROM device. | *6* | *K2* | *CO6* |
| | ii) | Derive a combinational circuit defined by the function, F1 = AB'C'+AB'C+ABC and F2 = A'BC+AB'C+ABC using PLA with minimal AND gates. | *7* | *K2* | *CO6* |

**PART - C (1 × 15 = 15 Marks)**

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|---|---|---|---|---|---|
| 16. | a) | Describe the procedure of converting 8421 to Gray code converter also, construct the converter using only NAND gates. | *15* | *K3* | *CO2* |
| | | **OR** | | | |
| | b) | Interpret the following Boolean Function using K-map and give the logic diagram using basic gates also NAND -NAND diagram.<br>$F(A, B, C, D) = \sum m(0,7,8,9,10,12) + \sum d(2,5,13)$ | *15* | *K3* | *CO2* |