| Reg. No. | | | | | | | | | | | | | | | | |
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| Question Paper Code | 13083 |
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**B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024**

Third Semester

**Electronics and Communication Engineering**

**20ECPC301 - DIGITAL ELECTRONICS**

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

**PART - A (MCQ) (20 × 1 = 20 Marks)**

Answer ALL Questions

| | | Marks | K – Level | CO |
|---|---|---|---|---|
| 1. | A+AB=A represents which law<br>(a) Associative (b) Idempotence (c) Commutative (d) Absorption | 1 | K1 | CO1 |
| 2. | The logic gate that provides high output for same inputs<br>(a) NOT (b) X-NOR (c) AND (d) XOR | 1 | K1 | CO1 |
| 3. | A five variable karnaugh map needs<br>(a) 32 squares (b) 33 squares (c) 34 squares (d) 35 squares | 1 | K1 | CO1 |
| 4. | If A and B are the inputs of a half adder, the sum is given by<br>(a) A EX-NOR B (b) A XOR B (c) A OR B (d) A AND B | 1 | K1 | CO2 |
| 5. | The limiting factor on a speed of parallel adder is<br>(a) Input delay (b) Carry propagation delay<br>(c) Input propagation delay (d) Output delay | 1 | K1 | CO2 |
| 6. | One that is not the outcome of magnitude comparator is<br>(a) a < b (b) a = b (c) a > b (d) a – b | 1 | K1 | CO2 |
| 7. | A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?<br>(a) Tristate (b) End around (c) Universal (d) Conversion | 1 | K1 | CO3 |
| 8. | A flip flop stores<br>(a) 10 bit of information (b) 1 bit of information<br>(c) 2 bit of information (d) 3-bit information | 1 | K1 | CO3 |
| 9. | The basic storage element in a digital system is<br>(a) T Flip flop (b) Counter (c) Multiplexer (d) Decoder | 1 | K1 | CO3 |
| 10. | A mod 10 asynchronous counter needs<br>(a) 4 J-K flip flop & 1 NAND gate (b) 3 J-K flip flop & 1 NAND gate<br>(c) 5 J-K flip flop & 1 NAND gate (d) 4 J-K flip flop &2 NAND gate | 1 | K1 | CO4 |
| 11. | How many different states does a 2-bit asynchronous counter have?<br>(a) 1 (b) 4 (c) 2 (d) 8 | 1 | K1 | CO4 |
| 12. | Essential Hazards exists only<br>(a) in unequal circuits (b) in sequential circuits<br>(c) in combinational circuits (d) in adder circuits | 1 | K1 | CO4 |
| 13. | The analysis of Asynchronous sequential circuits are used to obtain<br>(a) a table (b) a diagram (c) graph (d) both a and b | 1 | K1 | CO5 |
| 14. | The flow table which has exactly one stable state for each row in the table is called<br>(a) Race free table (b) Transition table (c) Essential table (d) None of the above | 1 | K1 | CO5 |
| 15. | The race in which stable state depends on order is called<br>(a) Critical race (b) Identical race (c) Non critical race (d) Defined race | 1 | K1 | CO5 |
| 16. | Which of the following sequential circuit generates the feedback path due to the cross coupled connection from the output of one gate to the input of another gate?<br>(a) Synchronous (b) Asynchronous (c) Excitation variable (d) Continuously change | 1 | K1 | CO5 |
| 17. | EPROM can be<br>(a) UVPROM (b) EEPROM (c) both a and b (d) None of the above | 1 | K1 | CO6 |

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|---|---|---|---|---|
| 18. | Which of the following is an example of volatile memory?<br>(a) ROM (b) RAM (c) PROM (d) Hard-disk | *1* | *K1* | *CO6* |
| 19. | PAL has<br>(a) Programmable AND & OR array (b) Programmable AND & Fixed OR array<br>(c) Fixed AND & Programmable OR array (d) None of the above. | *1* | *K1* | *CO6* |
| 20. | The ECL behaves as _____<br>(a) NOT gate (b) NOR gate (c) NAND gate (d) AND gate | *1* | *K1* | *CO6* |

**PART - B (10 × 2 = 20 Marks)**

Answer ALL Questions

| | | | | |
|---|---|---|---|---|
| 21. | State De Morgan's theorem. | *2* | *K1* | *CO1* |
| 22. | Convert binary 110111 into a decimal number system. | 2 | *K2* | *CO1* |
| 23. | Define Combinational logic circuit. | 2 | *K1* | *CO2* |
| 24. | Draw a 1:4 Demultiplexer using logic gates. | 2 | *K2* | *CO2* |
| 25. | Compute the minimum number of flip flop needed to design a counter of modulus 60. | 2 | *K2* | *CO3* |
| 26. | Write the characteristic equation of a SR Flip flop. | 2 | *K1* | *CO3* |
| 27. | Define Primitive flow table. | 2 | *K1* | *CO4* |
| 28. | What is pulse mode sequential circuit? | 2 | *K1* | *CO4* |
| 29. | List the advantages of FPGA. | 2 | *K1* | *CO5* |
| 30. | Compare PLA and PAL. | 2 | *K2* | *CO6* |

**PART - C (6 × 10 = 60 Marks)**

Answer ALL Questions

| | | | | | |
|---|---|---|---|---|---|
| 31. | a) | Apply Karnaugh Map method to reduce the following switching function and construct using NAND gates only. F(A,B,C,D)=∑m(1,3,5,8,9,11,15)+d(2,13). | *10* | *K3* | *CO1* |
| | | **OR** | | | |
| | b) | Use Quine Mccluskey method to simplify the given expression F(A,B,C,D)=∑m(0,2,3,5,7,9,11,13,14). | *10* | *K3* | *CO1* |
| 32. | a) | Explain with neat diagram the function of 4-bit binary parallel adder/ subtractor. | *10* | *K2* | *CO2* |
| | | **OR** | | | |
| | b) | With a neat diagram, explain in detail about the working of a 4 –bit look ahead carry adder. Also mention its advantage over conventional adder. | *10* | *K2* | *CO2* |
| 33. | a) | Explain Universal Shift Register and the principle of Operation of 4-bit Universal Shift Register. | *10* | *K2* | *CO3* |
| | | **OR** | | | |
| | b) | Illustrate the operation of master slave flip flop and show how the race around condition is eliminated. | *10* | *K2* | *CO3* |
| 34. | a) | Construct a synchronous counter that counts the sequence 000,001,010,011,100,101,110,111,000 using J K flip flop. | *10* | *K3* | *CO4* |
| | | **OR** | | | |
| | b) | With examples, explain Hazards and select suitable methods to detect and eliminate hazards. | *10* | *K3* | *CO4* |
| 35. | a) | Elaborate in detail about one hot state assignment and Summarize the design procedure for asynchronous sequential circuits. | *10* | *K2* | *CO5* |
| | | **OR** | | | |
| | b) | Describe about races and methods to eliminate races. | *10* | *K2* | *CO5* |

36. a) Use PLA to implement the following functions. *10 K3 CO6*

$A(x,y,z) = \sum m(1,2,4,6)$

$B(x,y,z) = \sum m(0,1,6,7)$

$C(x,y,z) = \sum m(2,6)$

**OR**

b) Construct a circuit to explain the operation of TTL. *10 K3 CO6*