Reg. No.															

Question Paper Code	13877

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Electronics and Communication Engineering

20ECPC301 - DIGITAL ELECTRONICS

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The implicants which will definitely occur in the final expression are called (a) redundant prime implicants (b) selective prime implicants (c) prime implicants (d) essential prime implicants	1	K1	CO1
2.	Minimize the expression using K-Map Y=A'B'C + A'BC + A'BC' + ABC + ABC' (a) Y=A+BC' (b) Y=B+A'C (c) Y=A+CD (d) Y=B+AC	1	K1	CO1
3.	How many AND, OR and EXOR gates are required for the configuration of full subtractor? (a) 1, 2, 2 (b) 3, 1, 2 (c) 4, 0, 1 (d) 2, 1, 2	1	K1	CO2
4.	Carry generator in full adder has expression (a) G=AB (b) G=A+B (c) G=A-B (d) G=A/B	1	K1	CO2
5.	A ring counter with 5 flip flops will have (a) 5 states (b) 10 states (c) 32 states (d) Infinite states	1	K1	CO3
6.	Placing an inverter between the inputs of S-R flip flop makes it a _____ flip flop. (a) T (b) D (c) J-K (d) Master slave	1	K1	CO3
7.	The number of flip flop required to build a Mod 15 counter is (a) 4 (b) 6 (c) 3 (d) 5	1	K1	CO4
8.	Following is not a Type of Hazard is (a) cycle (b) static 1 (c) static 0 (d) Dynamic	1	K1	CO4
9.	Table that is not a part of asynchronous analysis procedure is (a) Transition table (b) Flow table (c) Excitation table (d) State table	1	K1	CO5
10.	Number of address lines in EPROM 4096 X 8 is (a) 2 (b) 4 (c) 8 (d) 12	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Express the function Y=A+B'C in canonical POS.	2	K2	CO1
12.	Define Absorption Theorem.	2	K1	CO1
13.	Draw the full adder circuit using half adder.	2	K2	CO2
14.	Define priority Encoder.	2	K1	CO2
15.	Write the characteristic equation of a JK Flip flop.	2	K1	CO3
16.	Differentiate between the edge triggering and level triggering.	2	K2	CO3
17.	Draw Moore model circuit.	2	K2	CO4
18.	What is the advantage of state reduction in the design of sequential circuits?	2	K1	CO4
19.	Define critical race.	2	K1	CO5
20.	Define Cycle.	2	K1	CO5
21.	Differentiate Volatile and Non-Volatile memory.	2	K2	CO6
22.	Define Fan out.	2	K1	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Simplify using the K map method. f(A,B,C,D,E) =∑m (3,5,6,8,9,12,13,14,19,22,24,25,30)	11	K3	CO1
		OR			
	b)	Simplify using Quine McCluskey method. f(x1,x2,x3,x4,x5) =∑m(0,1,4,5,16,17,21,25,29)	11	K3	CO1
24.	a)	Draw a 1:8 demultiplexer and explain its operation in detail.	11	K2	CO2
		OR			
	b)	Illustrate a 4-bit Magnitude Comparator using logic gates with a neat diagram.	11	K2	CO2
25.	a)	Draw and explain the 4-bit SISO, SIPO, PISO and PIPO shift register with its waveforms.	11	K2	CO3
		OR			
	b)	Explain the design of Synchronous MOD -6 counter.	11	K2	CO3
26.	a)	Construct a synchronous counter that counts the sequence 000,001,010,011,100,101,110,111,000 using D flip flop.	11	K3	CO4
		OR			
	b)	Construct a static hazard free asynchronous circuit for the following switching function. f=Σm(1, 3, 6, 7)	11	K3	CO4
27.	a)	Construct an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input is transferred to Z. When Y is 0, the output does not change for any change in X.	11	K2	CO5
		OR			
	b)	Derive a primitive flow table for a circuit with two inputs x1 and x2 and two outputs z1 and z2 that satisfy the following four conditions: When x1x2 =00, the outputs z1z2 = 00 When x1 = 1 and x2 changes from 0 to 1, the output z1z2 =01 When x2 = 1 and x1 changes from 0 to 1, the output z1z2 =10 Otherwise, the output does not change.	11	K2	CO5
28.	a)	Explain the significance of FPGA with its advantages and applications.	11	K3	CO6
		OR			
	b)	Explain the operation of TTL with neat diagram.	11	K3	CO6