Reg. No.												

Question Paper Code	12342

B.E. / B.Tech - DEGREE EXAMINATIONS, NOV / DEC 2023

Third Semester

Electronics and Communication Engineering

20ECPC301 - DIGITAL ELECTRONICS

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level,CO
1.	State De-Morgan's theorem.	2,K1,CO1
2.	Infer the gray code of the binary value $[10101101]_2$.	2,K2,CO1
3.	Implement Boolean function F=Σm(1,2,3,7) using 3:8 decoder.	2,K2,CO2
4.	Draw the logic diagram for half subtractor.	2,K2,CO2
5.	How many flip flops are required for designing synchronous MOD 60 counter?	2,K2,CO3
6.	What is a shift register? Name different types of shift register?	2,K1,CO3
7.	Define Hazards. How it can be avoided?	2,K1,CO4
8.	Outline the characteristics of critical race.	2,K2,CO4
9.	Summarize the applications of PLA.	2,K2,CO6
10.	Draw the invertor circuit using CMOS.	2,K2,CO6

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Simplify the expression Y=Σm (7, 9, 10, 11, 12, 13, 14, 15) using the K map method.	13,K2,CO1
		OR	
	b)	Apply K Map method to reduce the following switching function and construct using NAND gates only. F(A, B, C, D) = Σm(0, 1, 5, 8, 9, 12, 13, 14, 15)	13,K3,CO1
12.	a)	Implement full adder with inputs x, y, z and two outputs S and C using multiplexer.	13,K3,CO2
		OR	
	b)	What is magnitude comparator? Design 2 bit Magnitude comparator and drive expression for A > B, A < B and A = B. Realize using gates.	13,K3,CO2
13.	a)	Design and explain the working of 4-bit parallel counter using T-flip flop. Draw its excitation table and state table.	13,K3,CO3

OR

b) Design a MOD 5 synchronous counter using JK flip flop and illustrate its timing diagram. *13,K3,CO3*

14. a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X. *13,K3,CO4*

OR

b) Construct a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0. Draw timing diagram, state diagram and Primitive flow table for designing the circuit. *13,K3,CO4*

15. a) Implement the following function using PAL *13,K3,CO6*
F_1 (A,B,C) = Σ(1,2,4,6) and F_2(A,B,C)=Σ(0,1,6,7).

OR

b) Illustrate the following Boolean functions using 8*2 PROM F_1=Σm(3,5,6,7) and F_2=Σm(1,2,3,4). *13,K3,CO6*

PART - C (1 × 15 = 15 Marks)

16. a) An asynchronous sequential has two internal states and one output. The excitation and output functions describing the circuit are *15,K2,CO5*

$Y_1 = x_1 x_2 + x_1 y_2' + x_2' y_1$

$Y_2 = x_2 + x_1 y_1' y_2 + x_1' y_1$

$Z = x_2 + y_1$

(i) Draw the logic diagram of the circuit.

(ii) Give the transition table and output map.

(iii) Give a flow table of the circuit.

OR

b) Compare fundamental mode and pulse mode circuits. Explain with an example transition table and flow table. *15,K2,CO5*