Reg. No.												

Question Paper Code	12398

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023

Fifth Semester

Electronics and Communication Engineering

20ECPC502 - VLSI DESIGN

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Write down the equation for describing the channel length modulation effect in NMOS transistors.	*2,K2,CO1*
2.	What is Logical effort of a gate?	*2,K1,CO1*
3.	Draw the footed Inverter.	*2,K2,CO2*
4.	What are skewed gates?	*2,K1,CO2*
5.	Define Clock Jitter.	*2,K1,CO3*
6.	List the properties of a Schmitt trigger.	*2,K1,CO3*
7.	Distinguish between == and === in Verilog.	*2,K2,CO4*
8.	What are compiler directives?	*2,K1,CO4*
9.	List out the components of data path.	*2,K1,CO5*
10.	State radix-2 booth encoding table.	*2,K1,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Draw the stick diagram and layout diagram for a three input NAND and NOR gates.	*13,K2,CO1*
		OR	
	b)	Describe the equation for source to drain current in three regions of operation of MOS Transistor and draw its IV Characteristics.	*13,K2,CO1*
12.	a)	Discuss the structure and working of pass transistor and transmission gate logic with neat diagrams.	*13,K2,CO2*
		OR	
	b)	Illustrate the following circuits in detail.	
		(i) Pseudo-nMOS,	*6,K2,CO2*
		(ii) Ganged CMOS.	*7,K2,CO2*

13. a) Explain the working principle of Astable and Monostable multivibrators. *13,K2,CO3*

OR

b) Explain about static power and dynamic power dissipation in detail. *13,K2,CO3*

14. a) Draw the logic diagram of a 4 to 1 MUX using logic gates and write a Verilog HDL code for the same in gate level modeling. *13,K3,CO4*

OR

b) Describe the three ways of specifying delays in continuous assignment statements. *13,K2,CO4*

15. a) Perform multiplication of -13 and 7 using Modified Booth Algorithm. *13,K3,CO5*

OR

b) Explain in detail the design of CMOS Static full adder circuit. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Discuss the various memory architectures in detail with neat diagrams. *15,K3,CO6*

OR

b) Construct a 4x4 NAND and NOR ROM array to store 1101,1001, 0001 and 1111. *15,K3,CO6*