Reg. No.								

Question Paper Code 13150

## B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Fifth Semester

## Electronics and Communication Engineering 20ECPC502 - VLSI DESIGN

Regulations - 2020

Du	ration: 3 Hours Ma	x. Mar	ks: 1	00				
	PART - A (MCQ) $(20 \times 1 = 20 \text{ Marks})$	Mauka	<i>K</i> –	co				
	Answer ALL Questions	Marks	Level	CO				
1.	The majority carriers of p-type semiconductor are:	1	K1	CO1				
	(a) Holes (b) Negative ions (c) Electrons (d) Positive ions							
2.	The oxide layer formed in the MOSFET is:	1	K1	CO1				
	(a) Metal oxide (b) Silicon dioxide (c) Poly Silicon oxide (d) Oxides of Non metals							
3.	nMOS devices are formed in	1	K1	CO1				
	(a) p-type substrate of high doping level (b) n-type substrate of low doping level							
	(c) p-type substrate of moderate doping level (d) n-type substrate of high doping level							
4.	In CMOS logic circuit the n-MOS transistor acts as:	1	<i>K1</i>	CO2				
_	(a) Load (b) Pull up network (c) Pull down network (d) Not used in CMOS circuits			~~*				
5.	In dynamic CMOS logic is used	1	KI	CO2				
_	(a) Two phase clock (b) Three phase clock (c) One phase clock (d) Four phase clock		W.1	GO2				
6.	In CMOS domino logic is possible	1	K1	CO2				
	(a) Inverting structure (b) Non inverting structure							
7	(c) Inverting and non inverting structure (d) Very complex design	1	V1	CO2				
7.	Inverting dynamic register element consists of transistors for nMOS and	1	ΚI	CO3				
	for CMOS.							
0	(a) Two, three (b) Three, two (c) Three, four (d) Four, three	1	<i>K1</i>	CO3				
8.	Clocked sequential circuits are  (a) Two phase everlapping clock.	1	KI	COS				
	(a) Two phase overlapping clock (b) Two phase non overlapping clock (c) Four phase overlapping clock (d) Four phase non overlapping clock							
Q	are the methods of sequencing static circuits.	1	<i>K1</i>	CO3				
٦.	(a) Flip flops (b) Pulsed Latches (c) 2 phase transparent latches (d) All of the above							
10	In Verilog, what is the purpose of the "always" block?	1	<i>K1</i>	CO4				
10.	(a) To declare variables (b) To instantiate modules							
	(c) To specify simulation time (d) To describe behavior using procedural statements							
11.	Which operator is used for concatenation in Verilog?	1	<i>K1</i>	CO4				
	(a) & (b)   (c) $^{\land}$ (d) {}							
12.	Which one of the following represents a hardware component in Verilog?	1	<i>K1</i>	CO4				
	(a) Module (b) Function (c) Loop (d) Variable							
13.	Multipliers are built using	1	K1	CO5				
	(a) binary adders (b) binary subtractions (c) dividers (d) multiplexers							
14.	Which of the following control signals has separate destinations?	1	K1	CO5				
	(a) ALU (b) Data Paths (c) System Bus (d) None of the above							
15.	Which method is easier to manipulate accumulator content?	1	<i>K1</i>	CO5				
	(a) left shifting (b) right shifting (c) serial shifting (d) parallel shifting							
16.	What does the control unit generate to control other units?	1	K1	CO5				
	(a) Transfer Signals (b) Command Signals (c) Control Signals (d) None of the above	1	V 1	COL				
17.	Which type of memory stores data currently being processed by the CPU?	1	ΚI	CO6				
	(a) Hard Drive (b) ROM (Read-Only Memory)							
	(c) RAM (Random Access Memory) (d) Cache Memory							

18.	Which statement is true about temporary data storage memory?  (a) It retains data even when the power is off.  (b) It is used for permanent data storage.					CO6							
	(c) It is used for archival purposes. (d) It is typically faster than hard drive storage. Which memory unit has the fastest access time? (a) Cache Memory (b) Hard Disk Drive (HDD) (c) Random Access Memory (RAM) (d) Solid State Drive (SSD)				K1	CO6							
20.	Whic (a) D	th of the following is used in main memory?  DDR (b) DRAM (c) SRAM	SRAM (d) PRAM										
	PART - B ( $10 \times 2 = 20 \text{ Marks}$ ) Answer ALL Questions												
21	Defin	Answer ALL Questions ne Stick Diagrams.		2	<i>K1</i>	CO1							
		ne Noise margin.		2	<i>K1</i>	CO1							
		ain Differential Pass Transistor Logic.		2	K2	CO2							
	-	ain Dual Rail Domino Logic.		2	K2	CO2							
25.	-	two applications of Monostable Sequential Circuits.		2	<i>K1</i>	CO3							
26.		is Clock Skew?		2	<i>K1</i>	CO3							
		is RTL in Verilog?		2	<i>K1</i>	CO4							
		is System Tasks?		2	<i>K1</i>	CO4							
		Ty how carry look-ahead adder decreases the propagation delay to	the least.	2	<i>K1</i>	CO5							
30. What is Non-Volatile READ-WRITE Memory?					<i>K1</i>	CO6							
		PART - C $(6 \times 10 = 60 \text{ Marks})$											
31.	۵)	Answer ALL Questions  Explain the DC transfer characteristic of CMOS invertor		10	K2	CO1							
31.	a)	Explain the DC transfer characteristic of CMOS inverter.  OR		10	112	001							
	b)	Discuss the CV characteristics of the CMOS.		10	K2	CO1							
32.	a)	Discuss in detail the characteristics of CMOS Transmission gas	tes.	10	K2	CO2							
	b)	Draw and explain the function of static CMOS.		10	K2	CO2							
33.	a)	Explain the static power dissipation in CMOS circuits with and expressions.	necessary diagrams	10	K2	CO3							
	1.	OR	at the state	10	W2	CO2							
	b)	Discuss in detail various pipelining approaches to optimize seq	uential circuits.	10	K2	CO3							
34.	a)	Write the Verilog HDL code of 8*1 Multiplexer using Gate Le	vel Modeling.	10	K3	CO4							
	b)	Construct a Verilog program for 2-bit magnitude comparat modelling.	or using data flow	10	К3	CO4							
35.	a)	Explain the design and operation of 4 x 4 multiplier circuit.  OR		10	K2	CO5							
	b)	Discuss the details about speed and trade off.		10	K2	CO5							
36.	a)	Explain the memory architecture and its control circuits in deta  OR	il.	10	K2	CO6							
	b)	Discuss Memory core its types in detail.		10	K2	CO6							