Reg. No.												

Question Paper Code	12863

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

Fifth Semester

Electronics and Communication Engineering

20ECPC502 - VLSI DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Why nMOS transistor is selected as pull down transistor?	2	K1	CO1
2.	Show the stick diagram of static CMOS 2 input NAND gate.	2	K1	CO1
3.	Show a 2 input XOR using nMOS pass transistor logic.	2	K2	CO2
4.	Discuss Ratioed circuits.	2	K2	CO2
5.	Describe Bistability principle.	2	K2	CO3
6.	Define Registers and Latches.	2	K1	CO3
7.	What are the data types used in Verilog HDL?	2	K1	CO4
8.	Discuss continuous assignment structure in Verilog.	2	K2	CO4
9.	Give example for some high-speed adders.	2	K2	CO5
10.	Classify the various memories used in IC design.	2	K2	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Explain in detail with a neat diagram about the DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation with neat diagram.	13	K2	CO1
		OR			
	b)	Discuss the layout design rules and draw diagrams for four input NAND and NOR gate.	13	K2	CO1
12.	a)	Develop Static and Dynamic power dissipation with relevant expressions.	13	K3	CO2
		OR			
	b)	Illustrate DCVSL logic with suitable example.	13	K2	CO2
13.	a)	Develop about CMOS register concept and design master slave triggered register, explain its operation with overlapping periods.	13	K3	CO3
		OR			

	b)	Illustrate the concept of timing issues and pipelining.	*13*	*K2*	*CO3*
14.	a)	Discuss and write Verilog module for 4-bit ripple carry adder with test bench.	*13*	*K2*	*CO4*
		OR			
	b)	Explain the compiler directives in detail.	*13*	*K2*	*CO4*
15.	a)	Discuss the concept of Carry look ahead adder in detail with relevant diagrams. Also mention its advantages and disadvantages.	*13*	*K2*	*CO5*
		OR			
	b)	Illustrate the product of +13 and -5 using booth algorithm.	*13*	*K2*	*CO5*

PART - C (1× 15 = 15 Marks)

16.	a)	Develop in detail about the array-structured memory architecture and the hierarchy memory architecture designs with neat diagrams.	*15*	*K3*	*CO6*
		OR			
	b)	Illustrate a 6T based SRAM Cell. Explain its read and write operations.	*15*	*K2*	*CO6*