Reg. No.												

Question Paper Code	12490

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023

Third Semester

Electrical and Electronics Engineering

20EEPC304 - DIGITAL LOGIC CIRCUITS

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	State the uses of Parity and Hamming Codes.	*2,K1,CO1*
2.	Compare RTL and DTL logic families.	*2,K2,CO1*
3.	List the applications of decoder and multiplexer.	*2.K1,CO2*
4.	Convert the given expression in canonical SOP form Y = AC + AB + BC.	*2,K2,CO2*
5.	Generalize the differences between combinational and sequential circuits.	*2,K2,CO3*
6.	Compare edge and level triggered FF.	*2,K2,CO3*
7.	Summarize the advantages and disadvantages of asynchronous sequential circuits.	*2,K2,CO4*
8.	Draw the block diagram of asynchronous sequential circuits.	*2,K1,CO4*
9.	List the types of PLD.	*2,K1,CO5*
10.	State the need for VHDL. List out the operators available in VHDL.	*2,K1,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Describe with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.	*13,K2,CO1*
		OR	
	b)	Explain the structure and working principle of TTL based Totem-pole output configuration.	*13,K2,CO1*
12.	a)	Minimize the following function using K-map: $F(A, B, C, D)=\sum m(0,4,6,8,9,10,12) +\sum d(2,13)$ and implement it using only NOR gates.	*13,K3,CO2*
		OR	
	b)	Design a 4-bit Binary to Gray code converter and implement it using EX-OR gates.	*13,K3,CO2*

13. a) Explain the operation of 4-bit PISO and SISO shift register. *13,K2,CO3*

OR

b) Explain the operation of JK Flip flop and T-Flip flop with state diagram, characteristic table and characteristics equation. *13,K2,CO3*

14. a) An asynchronous sequential circuit is described by the following excitation function, $Y=x_1x_2 +(x_1+x_2)y$ and output function $Z= y$. (i) Predict the logic diagram of the circuit. (ii) Interpret the transition table and the output map. (iii)Obtain its flow table. *13,K3,CO4*

OR

b) Implement the following logic and analyze for the presence of any hazard $f=x_1x_2 + x'_1x_3$. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. *13,K3,CO4*

15. a) Explain in detail the design procedure for register transfer language. *13,K2,CO5*

OR

b) Describe the modeling techniques available in HDL. Give the VHDL code to realize a full adder using Behavioural modeling. *13,K2,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Design a combinational circuit with three inputs x, y, z and the three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is one less than the input. *15,K3,CO2*

OR

b) Assess the VHDL code for Binary UP/DOWN counter using JK flip flops. *15,K3,CO5*