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Question Paper Code	13289
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B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Third Semester

Electrical and Electronics Engineering

20EPC304 - DIGITAL LOGIC CIRCUITS

Regulations - 2020

Duration: 3 Hours

Max. Marks: 100

PART - A (MCQ) (20 × 1 = 20 Marks)

Answer ALL Questions

	Marks	K – Level	CO
1. The decimal number 13 is represented in natural BCD as (a) 1101 (b) 0001 0011 (c) 00001101 (d) 00011101	1	K1	CO1
2. A XOR gate produces output only when the inputs are (a) High (b) Low (c) Different (d) Equal	1	K1	CO1
3. Extremely low power dissipation and low cost per gate can be achieved in the following IC (a) ECL (b) CMOS (c) TTL (d) MOS	1	K1	CO1
4. Which binary code is commonly used for error detection and correction in data transmission? (a) Gray code (b) BCD (c) Hamming code (d) Excess-3 code	1	K1	CO1
5. A data selector is also called as (a) Priority encoder (b) Multiplexer (c) Decoder (d) Demultiplexer	1	K1	CO2
6. How many AND gates are required for a 1-to-8 multiplexer? (a) 2 (b) 16 (c) 8 (d) 4	1	K1	CO2
7. If a three variable switching function is expressed as the product of maxterms by $f(A,B,C) = \Pi(0,3,5,6)$ then it can also be expressed as the sum of minterms by (a) $\Pi(1,2,4,7)$ (b) $\Sigma(0,3,5,6)$ (c) $\Sigma(1,2,4,7)$ (d) $\Sigma(1,2,3,7)$	1	K2	CO2
8. If A and B are the inputs of a half adder, the sum is given by _____ (a) A AND B (b) A OR B (c) A XOR B (d) A EX-NOR	1	K1	CO2
9. "No Change" condition in JK Flip Flop is when _____. (a) $J = 1, K = 1$ (b) $J = 1, K = 0$ (c) $J = 0, K = 1$ (d) $J = K = 0$	1	K2	CO3
10. The term synchronous means _____. (a) The output changes state only when any of the input is triggered (b) The output changes state only when the clock input is triggered (c) The output changes state only when the input is reversed (d) The output changes state only when the input follows it	1	K2	CO3
11. BCD counter is also known as _____. (a) Parallel counter (b) Decade counter (c) Synchronous counter (d) VLSI counter	1	K2	CO3
12. What is state diagram? (a) It provides the graphical representation of states (b) It provides exactly the same information as the state table (c) It is same as the truth table (d) It is similar to the characteristic equation	1	K2	CO3
13. Asynchronous sequential logic circuit not uses (a) input (b) output (c) clock pulses (d) time	1	K1	CO4
14. A ripple counter's speed is limited by the propagation delay of _____. (a) Each flip-flop (b) All flip-flops and gates (c) The flip-flops only with gates (d) Only circuit gates	1	K1	CO4
15. The race in which stable state does not depends on order is called (a) Critical race (b) Identical race (c) Non-critical race (d) Defined race	1	K1	CO4

16. The removal of hazards in combinational logic circuits requires the addition of redundantto the circuit. 1 K1 CO4
 (a) flip-flops (b) gates (c) Both flip flops and gates (d) latches
17. _____ is a collection of functions, procedure, variables, constants, types, attributes and components in VHDL. 1 K1 CO5
 (a) Process (b) package (c) functions (d) generic
18. Which type of PLD should be used to program basic logic functions? 1 K1 CO5
 (a) CPLD (b) PAL (c) PLA (d) SLD
19. The FPGA refers to.... 1 K1 CO5
 (a) First programmable Gate Array (b) Field Programmable Gate Array
 (c) First Program Gate Array (d) Field Program Gate Array
20. The OR array is in a PAL. 1 K1 CO5
 (a) Programmable (b) Fixed (c) Floating (d) Does not exist

PART - B (10 × 2 = 20 Marks)

Answer ALL Questions

21. Solve 9's complement of 432. 2 K3 CO1
22. Solve (2.B6)₁₆ into binary and octal. 2 K3 CO1
23. List the types of code convertors. 2 K1 CO2
24. Define minterm and maxterm. 2 K1 CO2
25. Choose the minimum number of flip flops required to design mod 20 counters. 2 K1 CO3
26. What are the types of triggering in a flip flop? 2 K2 CO3
27. Compare flow table and transition table. 2 K2 CO4
28. Define critical race. 2 K1 CO4
29. Define ROM. 2 K1 CO5
30. Develop a VHDL code for component AND. 2 K3 CO5

PART - C (6 × 10 = 60 Marks)

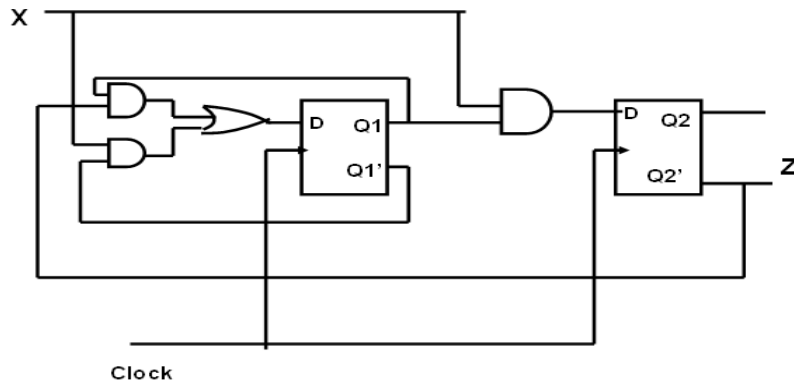
Answer ALL Questions

31. a) i) Compare Totem pole TTL and open collector TTL output configuration. 5 K2 CO1
 ii) Explain the operation of an open collector 2-input TTL NAND gate. 5 K2 CO1
- OR**
- b) Assume that the code word 1001100 is transmitted and that 1000100 is received. The receiver does not know what was transmitted and must look for proper parities to determine if the code is correct. Identify any error that has occurred in transmission if even parity is used. 10 K3 CO1
32. a) Solve the following Boolean function F , together with the don't-care conditions d, and then express the simplified function in sum of minterms: 10 K3 CO2
 a) $F(x, y, z) = \sum (0, 1, 2, 4, 5)$, $d(x, y, z) = \sum (3, 6, 7)$
 b) $F(A, B, C, D) = \sum (0, 6, 8, 13, 14)$, $dA, B, C, D) = \sum (2, 4, 10)$
 c) $F(A, B, C, D) = \sum (1, 3, 5, 7, 9, 15)$, $dA, B, C, D) = \sum (4, 6, 12, 13)$
- OR**
- b) Explain the operation of (i) Halfadder (ii) Full Adder circuits. 10 K2 CO2
33. a) Outline a synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip-flop. 10 K2 CO3

OR

b)

10 K2 CO3



For the given Moore model sequential circuit, Interpret the state table, state diagram, flip-flop input and output equations.

34. a) For the given boolean function, solve the hazard free circuit. 10 K3 CO4
 $F(A,B,C,D) = \sum m(1,3,6,7,13,15)$. Explain hazard in few words.

OR

- b) An asynchronous sequential circuit is described by the following excitation and output function, $Y = x_1 x_2 + (x_1 + x_2)y$ and $Z = y$. Model the logic diagram of the circuit, interpret the transition table and the output map. And also obtain its flow table. 10 K3 CO4

35. a) Develop VHDL code for 4 bit up and down counter. 10 K3 CO5

OR

- b) Explain the concept of operators and its types in detail. 10 K2 CO5

36. a) i) Develop an asynchronous sequential circuit with two inputs X and Y and with one output. Whenever Y is 1, input X is transferred to Z. Whenever Y is 0, the output does not change for any change in X. 5 K3 CO4

- ii) Develop a PLA defined by the functions $F1 = \sum m(3,5,7)$ and $F2 = \sum m(4,5,7)$. 5 K3 CO5

OR

- b) i) Explain critical and non-critical race. How will you obtain race free conditions? 5 K2 CO4

- ii) Develop VHDL code to realize Half Adder. 5 K3 CO5