B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Electrical and Electronics Engineering

20EEPC304 - DIGITAL LOGIC CIRCUITS

Regulations - 2020

Duration: 3 Hours   Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)
Answer ALL Questions

		Marks	K–Level	CO
1.	The binary equivalent of the decimal number 25 is: (a) 11001 (b) 10101(c) 11100(d) 10011	1	K1	CO1
2.	The logic family with lowest power consumption is: (a) TTL(b) CMOS(c) ECL(d) DTL	1	K1	CO1
3.	The number of minterms possible for n variables is: (a) n(b) 2n(c) 2^n(d) n^2	1	K2	CO2
4.	The borrow output in a half subtractor is given by: (a) $A'B$(b) AB'(c) $A \oplus B$(d) AB	1	K2	CO2
5.	The basic storage element in sequential logic is: (a) NAND gate(b) Flip-flop(c) Encoder(d) Decoder	1	K1	CO3
6.	A ripple counter is another name for: (a) Synchronous counter(b) Asynchronous counter (c) Ring counter(d) Modulo counter	1	K1	CO3
7.	Asynchronous sequential circuits do not use a (a) Clock signal(b) Flip-flop(c) Latch(d) Feedback path	1	K2	CO4
8.	To eliminate hazards, one can use (a) Redundant logic terms(b) Faster gates (c) Additional clocks(d) Reduced feedback	1	K2	CO4
9.	The FPGA stands for (a) Fixed Programmable Gate Array(b) Field Programmable Gate Array(c) Flexible Programmable Gate Array(d) Fast Programmable Gate Array	1	K1	CO5
10.	The VHDL code can be used to describe (a) Only hardware structure(b) Only behavior of the system (c) Both structure and behavior of hardware(d) Only software flow	1	K2	CO5

PART - B (12 × 2 = 24 Marks)
Answer ALL Questions

		Marks	K–Level	CO
11.	Explain the conversion of $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.	2	K2	CO1
12.	List the major characteristics of a digital logic family.	2	K1	CO1
13.	Define combinational circuit. How does it differ from a sequential circuit?	2	K1	CO2
14.	Compare between multiplexers and demultiplexers.	2	K2	CO2
15.	Compare between level triggering and edge triggering.	2	K2	CO3
16.	Define state diagram and state assignment in sequential circuit design.	2	K1	CO3
17.	What is a race condition? Classify the types of races.	2	K1	CO4
18.	List the different types of errors that occur in digital circuits.	2	K1	CO4
19.	Comparebetween PLA and PAL.	2	K2	CO5
20.	Summarize the advantages of VHDL simulation in digital system design.	2	K2	CO5
21.	Compare the difference between asynchronous and synchronous counters.	2	K2	CO3
22.	What is a flow table? How does it differ from a state table?	2	K1	CO4

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create   **14038**

PART - C (6 × 11 = 66 Marks)
Answer ALL Questions

23. a) Illustrate the methods of error detection and correction in digital communication systems.   *11*   *K2*   *CO1*

OR

   b) With neat circuit diagrams, Explainthe operation of an RTL (Resistor-Transistor Logic) gate. Discuss its advantages and disadvantages.   *11*   *K2*   *CO1*

24. a) Using Karnaugh maps,Illustratethe minimization of the following Boolean functions: *11*   *K2*   *CO2*
   (i) $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10, 14)$
   (ii) $F(A, B, C) = \Pi(1, 2, 4, 6)$

OR

   b) (i) Interpret the BCD-to-Excess-3 code converter with truth table and logic diagram.   *6*   *K2*   *CO2*

     (ii) Explain how a full adder can be constructed using two half adders and an OR gate.   *5*   *K2*   *CO2*

25. a) Experiment with the working of SR flip-flop using NAND and NOR gates. Derive its characteristic equation.   *11*   *K3*   *CO3*

OR

   b) (i) Identify the working of universal shift register and discuss its modes of operation.   *6*   *K3*   *CO3*

     (ii) Develop a synchronous 3-bit binary up counter using T flip-flops.   *5*   *K3*   *CO3*

26. a) An asynchronous sequential circuit is described by the following excitation and output function,   *11*   *K3*   *CO4*
   $Y=x1\ x2 +(x1+x2)y$
   $Z= y$
   (i) Model the logic diagram of the circuit.
   (ii) Utilize the transition table and the output map.
   (iii) Solve its flow table.

OR

   b) (i) Identify the hazards in asynchronous sequential circuits.   *6*   *K3*   *CO4*

     (ii) Develop a hazard-free logic circuit for $F(A, B, C) = A'B + BC$ using consensus terms.   *5*   *K3*   *CO4*

27. a) Show the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions.   *11*   *K2*   *CO5*
   $F_1(A,B,C)= \sum (0, 1, 2, 4)$
   $F_2(A,B,C)=\sum (0, 5, 6, 7)$

OR

   b) Explain about Operators in VHDL. Write a VHDL code for half adder circuit.   *11*   *K2*   *CO5*

28. a)(i) Interpret the logical expression using K-map in SOP form : $F (A, B, C, D) =\sum m (0, 2, 3, 6, 7) + d (8, 10, 11, 15)$.   *6*   *K2*   *CO2*

     (ii) Outline the logical expression: $ABCD + AB'C'D' + AB'C + AB$ on a 4 variable K-map; obtain the simplified expression from the map.   *5*   *K2*   *CO2*

OR

   b) (i) Explain by implementing the following Boolean function using a 4-to-1 MUX $F(A, B, C) = \Sigma(1, 3, 5, 7)$.   *6*   *K2*   *CO2*

     (ii) Illustrate a 1-to-8 demultiplexer using two 1-to-4 demultiplexer.   *5*   *K2*   *CO2*

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create   **14038**