Reg. No.															

Question Paper Code	12915

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

Third Semester

Electrical and Electronics Engineering

20EEPC304 - DIGITAL LOGIC CIRCUITS

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Design AND gate using only NAND gates.	2	K2	CO1
2.	Apply De-Morgan's theorem to simplify (A'+ BC')'.	2	K2	CO1
3.	Write the Standard canonical POS form of F=A.(A+B').	2	K2	CO2
4.	List the applications of Multiplexer.	2	K1	CO2
5.	Differentiate latch and flip flop.	2	K2	CO3
6.	Give characteristic equation for D and T flip flops.	2	K2	CO3
7.	Explain Dynamic Hazard.	2	K1	CO4
8.	Define critical race.	2	K1	CO4
9.	Draw the general architecture of CPLD.	2	K1	CO5
10.	Explain the declaration of entity in VHDL.	2	K1	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

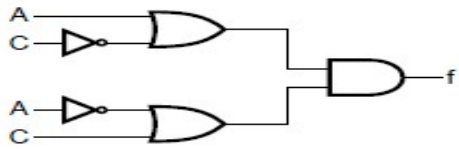
			Marks	K – Level	CO
11.	a)	Explain the operation of DTL with suitable example.	13	K2	CO1
		OR			
	b) i)	Find the hexadecimal equivalent of the decimal number 256 and the octal equivalent of the decimal number 64.	6	K3	CO1
	ii)	Assume that the code word 1001100 is transmitted and that 1000100 is received. The receiver does not know what was transmitted and must look for proper parities to determine if the code is correct. Designate any error that has occurred in transmission if even parity is used.	7	K3	CO1
12.	a) i)	Implement the following Boolean functions, using Suitable Multiplexer: $F(w, x, y, z) = \sum (2, 3, 10, 11, 12, 13, 14, 15$	6	K3	CO2
	ii)	Design and explain the operation of Half adder.	7	K4	CO2
		OR			

b) i)	Design and Explain the operation of Binary to excess-3 code convertor.	6	K4	CO2
ii)	Implement full adder using DEMUX.	7	K3	CO2

13.	a)	Demonstrate 3 bit Asynchronous down counter using JK flipflop.	13	K2	CO3
		OR			
	b)	Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary' input is 4, 5, 6, or 7, the binary output is one less than the input.	13	K4	CO3

14.	a)	Design hazard free circuit for the following: $F(A,B,C,D)=\sum(2,5,6,7,10,13,15)$	13	K4	CO4
		OR			
	b)	Design a pulse mode circuit with inputs x1,x2. one output z. The circuit should produce an output pulse to coincide with the last input pulse in the sequence x1-x2-x2. No other input sequence should produce an output pulse. Use T flipflops.	13	K4	CO4

15.	a)	Build a VHDL code to realize full adder in dataflow modelling, behavioural and structural modelling.	13	K3	CO5
		OR			
	b)	Develop VHDL code for the circuit shown:	13	K4	CO5



PART - C (1 × 15 = 15 Marks)

16.	a) i)	Implement the following using PAL:- $A=\sum m(1,2,4,6)$; $B=\sum m(0,1,3,6,7)$ $C=\sum m(1,2,4,6,7)$; $D=\sum m(1,2,3,5,7)$	8	K3	CO5
	ii)	Minimize using K-Map: $F(A, B, C, D) = \sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	7	K3	CO2
		OR			
	b) i)	Convert the following: $(56)_{10}$ = (_____?____)$_8$ $(223)_{10}$ = (____?_____)$_{16}$	8	K3	CO1
	ii)	An asynchronous sequential circuit is described by the following excitation and output function, Y=x1 x2 +(x1+x2)y Z= y Predict the logic diagram of the circuit, Interpret the transition table and the output map, Obtain its flow table.	7	K3	CO4