Reg. No.

Question Paper Code 13242

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Fifth Semester

Electrical and Electronics Engineering 20EEPC503 - MICROPROCESSORS AND MICROCONTROLLERS

Regulations - 2020

Dι	uration: 3 Hours Max	. Marl	ks: 10	00
$PART - A (MCQ) (20 \times 1 = 20 Marks)$				
	Answer ALL Questions	Marks	Level	co
1.	The accumulator in the 8085 is a/an bit register.	1	<i>K1</i>	CO1
	(a) 8 (b) 16 (c) 32 (d) 64			
2.	During the execution of an instruction in 8085, the machine cycle starts with which	. 1	K1	CO1
	operation?			
	(a) Opcode Fetch (b) Memory Read (c) Memory Write (d) I/O Read			
3.	In a typical memory read cycle of the 8085, how many clock cycles are required?	1	K1	CO1
	(a) 1 clock cycle (b) 2 clock cycles (c) 3 clock cycles (d) 4 clock cycles	1	17.1	CO.1
4.		1	KI	CO1
_	(a)Flags (b) Address register (c) Program counter (d) Accumulator	1	V1	CO2
5.	Which of the following is a 3-byte instruction in 8085?	1	K1	CO2
6	(a) MOV A, B (b) JMP 2050H (c) CPI 32H (d) ANI 0FH	1	<i>K1</i>	CO2
6.	What is the function of the instruction CPI 45H in the 8085?	1	KI	CO2
	(a) Compares the accumulator with 45H (b) Adds 45H to the accumulator (c) Subtracts 45H from the accumulator (d) Loads 45H into the accumulator			
7.	Which of the following is a control instruction in the 8085?	1	K1	CO2
7.	(a) STA (b) HLT (c) MOV (d) MVI	•		002
8.	The instruction XCHG in the 8085 microprocessor exchanges data between which	1	<i>K1</i>	CO2
0.	registers?			
	(a) A and B (b) A and H (c) HL and DE (d) BC and DE			
9.	In the 8254 timer, Mode 3 is also known as:	1	<i>K1</i>	CO3
	(a) Interrupt on Terminal Count (b) Rate Generator			
	(a) Interrupt on Terminal Count (b) Rate Generator (c) Square Wave Generator (d) Software Triggered Strobe			
10.	Stores the bits required to mask the interrupt input.	1	K1	CO3
	(a) IRR (b) ISR (c) IMR (d) NMI			
11.	The 8-bit data buffer interfaces internal circuit of 8253 to microprocessor	. 1	K1	CO3
	systems bus			
	(a) Unidirectional (b) Single (c) Bidirectional (d) None of these			
12.	In which of the following modes is the 8255 PPI capable of transferring data while	1	<i>K1</i>	CO3
	handshaking with the interfaced device?			
1.0	(a) BSR mode (b) Mode 0 of I/O mode (c) Mode 1 of I/O mode (d) Mode 2 of I/O mode	1	17.1	GO 1
13.	Which of the following ports can be used as both input and output in the 8051?	1	KI	CO4
1.4	(a) Port 0 (b) Port 1 (c) Port 2 (d) All of the above	1	V1	CO4
14.	The matrix keypad in the 8051 consists of	1	ΛI	C <i>O</i> 4
	(a) Rows and columns of switches (b) Rows of resistors (c) Picital display LEDs			
15	(c) Digital display LEDs (d) Analog inputs Which of the following has the highest priority in the 8051 interrupt system?	1	<i>K1</i>	CO4
13.	Which of the following has the highest priority in the 8051 interrupt system? (a) External Interrupt 0 (b) Timer 1 interrupt	1	11.1	001
	(a) External Interrupt 0 (b) Timer 1 interrupt (c) Serial communication interrupt (d) Reset			
16	Which bit is used to start or stop Timer 0 in the 8051?	1	<i>K1</i>	CO4
10.	(a) TR0 (b) TF0 (c) IE0 (d) TMOD			
	(a) 1110D			

17.	Which of the following is a typical use case for ARM Cortex-M0 processors? (a) Internet of Things (IoT) devices (b) High-performance servers (c) Desktop PCs (d) Supercomputers	1	K1	CO5
18.	Which tool is typically used to compile source code for the ARM Cortex-M0? (a) GCC ARM Compiler (b) Keil uVision (c) IAR Embedded Workbench (d) All of the above	1	K1	CO5
19.	The "endian" used by the ARM Cortex-M0 can be configured as: (a) Big-endian only (b) Little-endian only	1	K1	CO5
20.	The Cortex-M0 microcontroller uses which of the following to interface with external memory and peripherals?	1	K1	CO5
	 (a) APB (Advanced Peripheral Bus) (b) AHB (Advanced High-performance Bus) (c) AMBA (Advanced Microcontroller Bus Architecture) (d) AXI (Advanced eXtensible Interface 			
	$PART - B (10 \times 2 = 20 Marks)$			
	Answer ALL Questions			aa.
	Show the function of the signal IO/M, S0, S1.	2	K1	CO1
	Outline Program counter in 8085 mp.	2	K2	CO1
	If the clock frequency is 5 MHz, show the time required to execute an instruction having 18 T-states.	2	K2	CO2
	Relate the similarity and difference between compare and subtract instructions.	2	K2	CO2
	What is the need for 8259 PIC?	2	K1	CO3
26.	Compare the two key lockout and N-key rollover modes in 8279.	2	<i>K2</i>	CO3
27.	List the interrupts of 8051 microcontroller.	2	<i>K1</i>	CO4
28.	Illustrate the function of Program Status Word in microcontrollers.	2	<i>K2</i>	CO4
29.	What is M0 ARM cortex?	2	K1	CO5
30.	List some applications of ARM cortex.	2	K1	CO5
	PART - C $(6 \times 10 = 60 \text{ Marks})$ Answer ALL Questions			
31.	a) Explain with a neat block diagram the architecture of 8085 microprocessor.	10	K2	CO1
	OR			
	b) Outline the timing diagram for memory read and write operations and explain.	10	K2	CO1
32.	a) Identify the various addressing modes of 8085 microprocessor with suitable example. OR	10	К3	CO2
	b) Develop an ALP of 8085 microprocessor to add 16 bit data stored in memory from 9200H.	10	К3	CO2
33.	a) Explain the architecture, functions and modes of the 8255 PPI. OR	10	K2	CO3
	b) Discuss briefly the block diagram of 8254 timer.	10	K2	CO3
34.	 a) Explain with a neat block diagram the architecture of 8051 microcontroller. OR 	10	K2	CO4

	b)	Explain the stepper motor control using 8051 and write an assembly language program for running the stepper motor in clockwise direction.	10	K2	CO4
35.	a)	Discuss in detail about programming model of ARM M0 cortex.	10	K2	CO5
		OR			
	b)	Show ARM Development flow with help of a diagram.	10	K2	CO5
36.	a) i)	Summarize the addressing modes of 8051 microcontroller with suitable examples.	5	K2	CO4
	ii)	Explain the concept of ARM cortex M0.	5	K2	CO5
		OR			
	b) i)	Explain the following instructions of 8051 micro-controller	5	K2	CO4
		1. DJNZ Ro, HERE			
		2. CJNZ @ Ri, #data, rel			
	ii)	Summarize the evolution and main trends of the microcontroller market until the	5	K2	CO5
		appearance of ARM Cortex core micro controllers.			