Reg. No.																

Question Paper Code	14313

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2026

Eighth Semester

Electronics and Instrumentation Engineering

20EIEL803 - VLSI DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (i) (MCQ)
(16 × 1 = 16 Marks)
Answer ALL Questions

		Marks	K – Level	CO
1.	To obtain full output voltage swing in an inverter, Choose which transistor configuration should be used? a) Two NMOS b) Two PMOS c) One NMOS + One PMOS d) BJT pair	1	K3	CO1
2.	Select the one : The main limitation of NMOS pass transistor arises due to: a) High switching delay b) Threshold voltage drop across the transistor c) Increased capacitance d) Low current drive	1	K2	CO1
3.	Elmore delay is used for a) Power analysis b) Delay estimation c) Noise d) Area	1	K1	CO1
4.	Dynamic power depends on: a) Resistance b) Switching activity c) Area d) Delay	1	K1	CO2
5.	Domino logic avoids: a) High speed b) Cascading problems c) Voltage drop d) Static power	1	K2	CO2
6.	A designer wants low power with no static current flow. Which logic is best? a) Ratioed b) Static CMOS c) Dynamic d) Pass transistor	1	K3	CO2
7.	Sense amplifier is mainly used for: a) Power reduction b) Signal amplification c) Fast data detection d) Delay reduction	1	K1	CO3
8.	Choose the one: Static latches consume more power because: a) They switch faster b) Continuous current flow exists c) They use capacitors d) They use clocks	1	K2	CO3
9.	A circuit suffers from noisy input transitions. Which circuit is best to stabilize output? a) Latch b) Flip-flop c) Schmitt trigger d) Register	1	K3	CO3
10.	A Datapath consists of: a) Only memory b) Arithmetic and logic units c) Only control unit d) Sensors	1	K1	CO4
11.	Ripple carry adder is slow because: a) High power b) Sequential carry propagation c) Large area d) Low voltage	1	K2	CO4

12.	A system requires high-speed addition. Which adder is suitable?		1	K3	CO4
	a) Ripple carry adder	b) Carry look-ahead adder			
	c) Half adder	d) Serial adder			
13.	FPGA interconnects are used for:		1	K1	CO5
	a) Storage	b) Routing signals			
	c) Amplification	d) Power control			
14.	Scan design improves testability by:		1	K2	CO5
	a) Increasing speed	b) Converting sequential circuits to combinational for testing			
	c) Reducing area	d) Reducing power			
15.	A chip must test itself without external equipment. Which method is used?		1	K3	CO5
	a) Scan design	b) BIST			
	c) IDDQ	d) Routing			
16.	To detect leakage current faults in CMOS circuits, which method is used?		1	K3	CO5
	a) BIST	b) Scan testing			
	c) IDDQ testing	d) Boundary scan			

PART - A (ii) (Short Answer Questions)
(8 × 3 = 24 Marks)
Answer ALL Questions

17.	Construct the 3-input NAND gate using CMOS logic with truth table.	3	K3	CO1
18.	Examine long-channel I-V characteristics to identify regions of MOSFET operation.	3	K4	CO1
19.	Construct a stick diagram for a CMOS inverter.	3	K3	CO2
20.	Examine transmission gates to implement a multiplexer.	3	K4	CO2
21.	Construct the performance differences of pulse registers and static registers.	3	K3	CO3
22.	Model the role of shifters in improving processor performance.	3	K3	CO4
23.	Examine how memory core and peripheral circuitry interact during write operation.	3	K4	CO4
24.	Identify the differences between various FPGA interconnect routing procedures.	3	K3	CO5

PART - B (Descriptive Answer Questions)
(5 × 12 = 60 Marks)
Answer ALL Questions

25.	a)	Develop a CMOS inverter and explain its DC transfer characteristics with suitable diagrams.	12	K3	CO1
		OR			
	b)	Apply scaling concepts in MOS technology to explain its impact on performance and power.	12	K3	CO1
26.	a)	Analyze different low power techniques in CMOS circuits.	12	K4	CO2
		OR			
	b)	Compare CPL, DCVSPG, and DPL logic styles.	12	K4	CO2
27.	a)	Build True single phase clocked register design and explain its behavior.	12	K3	CO3
		OR			
	b)	Apply timing classification concepts to analyze a digital system with clock skew and delay.	12	K3	CO3
28.	a)	Examine 4 X 4 array type multiplier and find its criticalpath delay	12	K4	CO4

OR

	b)	Analyze the operation of Carry Bypass adders with neat diagram.	*12*	*K4*	*CO4*
29.	a)	Analyze the goals and objectives of (a) Floor planning (b) Placement (c) Routing in VLSI design.	*12*	*K4*	*CO5*

OR

	b)	Examine the Boundary Scan technique and explain its role in testing with diagrams.	*12*	*K4*	*CO5*