Reg. No.																

Question Paper Code	13070

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Fourth Semester

Electronics and Instrumentation Engineering

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (20 × 1 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	What is the decimal equivalent of binary 1011? (a) 9 (b) 10 (c) 11 (d) 12	1	K1	CO1
2.	In a 7-bit Hamming code, how many parity bits are there? (a) 1 (b) 2 (c) 3 (d) 4	1	K2	CO1
3.	The Boolean expression for A + A'B simplifies to: (a) A + B (b) A' + B (c) A'B (d) AB	1	K2	CO1
4.	In a 3-variable K-map, how many cells are there? (a) 2 (b) 4 (c) 8 (d) 16	1	K1	CO1
5.	In digital electronics, which logic gate produces a 1 output only if all inputs are 1? (a) OR (b) AND (c) XOR (d) NOT	1	K1	CO2
6.	In a binary to Gray code converter, what happens to the most significant bit? (a) It remains unchanged (b) It is complemented (c) It is shifted left (d) It is shifted right	1	K2	CO2
7.	Which of the following is a characteristic of a demultiplexer? (a) Converts single input to multiple outputs (b) Multiple inputs to one output (c) Parallel to serial data conversion (d) Stores digital data	1	K1	CO2
8.	Which of the following is a combinational logic circuit? (a) Flip-flop (b) Counter (c) Adder (d) Register	1	K1	CO2
9.	A 4-bit ring counter requires how many flip-flops? (a) 3 (b) 4 (c) 5 (d) 6	1	K2	CO3
10.	Which type of shift register can perform serial and parallel operations? (a) Universal shift register (b) Ring counter (c) Johnson counter (d) Decade counter	1	K1	CO3
11.	In a JK flip-flop, what is the output when J=1 and K=1? (a) No change (b) Set (c) Reset (d) Toggle	1	K2	CO3
12.	The maximum count of a 4-bit asynchronous counter is (a) 15 (b) 16 (c) 10 (d) 8	1	K2	CO3
13.	Which of the following is a type of asynchronous hazard? (a) Logical hazard (b) Static hazard (c) Dynamic hazard (d) All of the above	1	K1	CO4
14.	A race condition in an asynchronous circuit (a) A condition where the circuit races through multiple outputs (b) A situation where the output depends on the sequence of changing inputs (c) A stable state of the circuit (d) An error-free condition in asynchronous circuits	1	K2	CO4
15.	Which PLD is the simplest and is only programmable in its AND array? (a) PLA (b) PROM (c) PAL (d) CPLD	1	K1	CO4

16.	The main difference between CPLD and FPGA is (a) FPGAs are used for simple circuits, while CPLDs are for complex circuits (b) CPLDs have a higher density of logic resources than FPGAs (c) FPGAs are more flexible and reconfigurable than CPLDs (d) CPLDs are faster than FPGAs for all applications	*1*	*K2*	*CO4*
17.	Which of the following is a primary data type in VHDL? (a) Bit (b) Float (c) Integer (d) String	*1*	*K1*	*CO5*
18.	What would be the output of a 4-bit synchronous counter after 10 clock pulses if it starts at 0000? (a) 0101 (b) 1010 (c) 1100 (d) 1011	*1*	*K2*	*CO5*
19.	The code given belongs to which of the following flip flop? library IEEE; use IEEE.std_logic_1164.all; entity ff is port(D,Clk : IN std_logic; Q: OUT std_logic); end ff; (a) SR flip flop (b) JK flip flop (c) D flip flop (d) None of the mentioned	*1*	*K2*	*CO5*
20.	Which construct is used to describe a combinational circuit in VHDL? (a) Process (b) Architecture (c) Entity (d) Signal	*1*	*K1*	*CO5*

PART - B (10 × 2 = 20 Marks)

Answer ALL Questions

21.	State De-Morgan's law.	*2*	*K1*	*CO1*
22.	Illustrate the steps to implement OR gate using NAND gate.	2	*K2*	*CO1*
23.	List two examples of combinational logic circuits.	2	*K1*	*CO2*
24.	Explain the main function of a half-adder.	2	*K2*	*CO2*
25.	Reproduce T flip flop using JK flip flop.	2	*K1*	*CO3*
26.	Enumerate the characteristics of different types of flip-flops.	2	*K2*	*CO3*
27.	Illustrate the various steps involved for designing asynchronous sequential circuits.	2	*K2*	*CO4*
28.	Outline the causes of essential Hazard.	2	*K1*	*CO4*
29.	Define Behavioral model.	2	*K1*	*CO5*
30.	Differentiate a signal and a variable.	2	*K2*	*CO5*

PART - C (6 × 10 = 60 Marks)

Answer ALL Questions

31.	a)	Explain the K-map method for simplifying Boolean expressions. Illustrate with a 4-variable Boolean function.	*10*	*K2*	*CO1*
		OR			
	b)	Explain with a out the advantages over other logic families. Neat diagram the operation of 2 input CMOS NAND gate and list.	*10*	*K2*	*CO1*
32.	a)	Design a full adder using 2 half adders.	*10*	*K3*	*CO2*
		OR			
	b)	Design a Gray to Binary code converter and implement the same using logic gates.	*10*	*K3*	*CO2*
33.	a)	Design and implement MOD-5 up counter using T Flip-flop.	*10*	*K3*	*CO3*
		OR			
	b)	Explain the circuit of a SR flipflop and explain its operation. Give the truth table, characteristic table and excitation table.	*10*	*K2*	*CO3*

34.	a)	Design an Asynchronous sequential circuit that has two inputs X1 and X2 and one output Z. When X1= 0, the output Z is 0. The first change in X2 that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to 0.	*10*	*K3*	*CO4*
		OR			
	b)	Explain in detail about critical races and non-critical races in asynchronous sequential circuits with examples.	*10*	*K2*	*CO4*
35.	a)	Design a logic circuit and write a VHDL program to add 3 bit numbers.	*10*	*K3*	*CO5*
		OR			
	b)	Construct the behavioral and structural model of a 1 to 4 demux.	*10*	*K3*	*CO5*
36.	a) i)	Describe the steps involved in the design of an asynchronous sequential circuit.	*5*	*K2*	*CO4*
	ii)	Write the behavioral model of a Full Subtractor.	*5*	*K2*	*CO5*
		OR			
	b) i)	Explain the concept and working of PROM.	*5*	*K2*	*CO4*
	ii)	Write a VHDL behavior descriptions of D flip flop.	*5*	*K2*	*CO5*