Reg. No.															

Question Paper Code	14257

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Fourth Semester

Electronics and Instrumentation Engineering

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	A digital circuit receives a BCD input 1001 (9). If 3 is added in binary, what will be the corrected BCD output? (a) 0000 with carry 1 (b) 1100 (c) 0010 0001 (d) 0001 0010	1	K2	CO1
2.	If a 7-bit Hamming code is used to transmit 4 data bits, and the received code is 1011011, which bit position has the error? (a) 2 (b) 3 (c) 5 (d) No error	1	K1	CO1
3.	The Boolean function $F(A,B,C) = A'B + AB' + ABC$ simplifies to (a) $A \oplus B$ (b) $A + B$ (c) $A \cdot B'$ (d) $A' + B'$	1	K1	CO2
4.	The circuit that performs A – B can be realized using (a) Full adder with B inputs inverted and Cin = 0 (b) Full adder with B inputs inverted and Cin = 1 (c) Encoder circuit (d) Decoder circuit	1	K2	CO2
5.	A JK flip-flop can function as a T flip-flop when (a) J = 1, K = 0 (b) J = K = 1 (c) J = K = 0 (d) J = 0, K = 1	1	K2	CO3
6.	A 4-bit synchronous counter has how many possible states? (a) 4 (b) 8 (c) 16 (d) 32	1	K1	CO3
7.	A race condition occurs when (a) Two or more inputs change simultaneously (b) The circuit is clocked synchronously (c) The propagation delay is zero (d) Flip-flops are edge triggered	1	K1	CO4
8.	A PROM has (a) Programmable AND and fixed OR arrays (b) Fixed AND and programmable OR array (c) Both arrays programmable (d) Both arrays fixed	1	K2	CO4
9.	In VHDL, which part of the design specifies how a circuit behaves rather than what components it contains? (a) Entity declaration (b) Architecture body (c) Library clause (d) Configuration specification	1	K1	CO5
10.	Which of the following is a primary data type in VHDL? (a) Bit (b) Float (c) Integer (d) String	1	K2	CO5

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Convert the Boolean function $F = A'B + AB' + AB$ into minimal SOP form using a K-map.	2	K1	CO1
12.	What is noise margin, and why is it important in digital circuits?	2	K2	CO1
13.	Apply De Morgan's theorem to simplify $(AB + C)'$.	2	K1	CO2
14.	Implement $F = AB + A'C$ using only NAND gates.	2	K2	CO2
15.	What is meant by propagation delay in a flip-flop?	2	K2	CO3
16.	Why is state reduction important in designing sequential circuits?	2	K2	CO3

17.	Differentiate synchronous and asynchronous sequential circuits.		*2*	*K2*	*CO4*
18.	Mention any two techniques to avoid race conditions in asynchronous circuits.		*2*	*K2*	*CO4*
19.	Define signal and variable in VHDL.		*2*	*K1*	*CO5*
20.	What is the use of the library IEEE and package std_logic_1164?		*2*	*K2*	*CO5*
21.	Reproduce T flip flop using JK flip flop.		*2*	*K2*	*CO3*
22.	What is the main difference between Moore and Mealy models of sequential circuits?		*2*	*K2*	*CO3*

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Obtain a simplified expression for the following Boolean functions using K-map. $F(A,B,C,D,E) = \sum m(0,1,4,5,16,17,21,25,29) + \sum d(6,7,22,26)$.	*11*	*K2*	*CO1*
		OR			
	b)	Compare Transistor-Transistor Logic and Emitter-Coupled Logic families in terms of Propagation delay, Power consumption, Noise margin, Fan-out.	*11*	*K2*	*CO1*
24.	a)	Write the truth table of a full adder and draw its logic diagram. Also construct full adder using two half adders and OR gate.	*11*	*K3*	*CO2*
		OR			
	b)	Design a Binary-to-Gray code converter and implement it using logic gates.	*11*	*K3*	*CO2*
25.	a)	Explain the operation of a JK flip-flop with truth table, excitation table, and logic Diagram. Compare its operation with an SR flip-flop and discuss how the JK flip-flop resolves the invalid state present in the SR flip-flop.	*11*	*K3*	*CO3*
		OR			
	b)	Design a synchronous counter using D flip flops that counts the given sequence 000,011,110,111,011,000, ...	*11*	*K3*	*CO3*
26.	a)	A combinational logic circuit is given by the expression F (A, B, C) = A^1B + BC (i) Draw the logic circuit for the given function. (ii) Identify the type(s) of hazards present in the circuit. (iii) Show how the circuit can be modified to make it hazard-free.	*11*	*K3*	*CO4*
		OR			
	b)	Implement the full adder circuit using PLA by deriving the PLA programming table.	*11*	*K3*	*CO4*
27.	a)	Design a MUX in VHDL using structural modeling.	*11*	*K3*	*CO5*
		OR			
	b)	Design a 4-bit synchronous up-down counter in VHDL.	*11*	*K3*	*CO5*
28.	a)	Explain in detail the usage of hamming codes for error detection and error correction with an example, considering the data bits as 1101and check whether code is correct or not.	*11*	*K3*	*CO1*
		OR			
	b)	Describe the operating characteristics of ECL logic families, including their typical applications in digital circuits.	*11*	*K3*	*CO1*