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Question Paper Code	14741

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2026

Fourth Semester

Electronics and Instrumentation Engineering

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART – A (i) (MCQ)
(16 × 1 = 16 Marks)
Answer ALL Questions

		Marks	K – Level	CO
1.	The hexadecimal number 2A in binary is: a) 101010 b) 111000 c) 110101 d) 111111	1	K1	CO1
2.	A Hamming code that can detect up to two errors and can correct one error is: a) Single-error correction code b) Double-error correction code c) Triple-error correction code d) None of the above	1	K1	CO1
3.	In a K-map, the pair can be combined if the terms are adjacent inthe same row is a) Vertically adjacent b) Horizontally adjacent c) Diagonally adjacent d) None of the above	1	K2	CO1
4.	A combinational logic circuit a) Flip-flop b) Counter c) Adder d) Register	1	K1	CO2
5.	In digital electronics, the logic gate which produces a 1 output with fall inputs are 1 is: a) OR b) AND c) XOR d) NOT	1	K1	CO2
6.	The main limitation of a half-adder a) Cannot handle more than one-bit b) Cannot handle carry input c) Slow operation speed d) Requires a high number of gates	1	K2	CO2
7.	A flip-flop is created by connecting T = 1 to a JK flip-flop. a) SR flip-flop b) Toggle flip-flop c) D flip-flop d) Master-Slave	1	K1	CO3
8.	A Mod-10 counter is also known as a: a) Ring counter b) Decade counter c) Binary counter d) Johnsoncounter	1	K1	CO3
9.	The type of shift register that can perform serial and paralleloperations a) Universal shift register b) Ring counter c) Johnson counter d) Decade counter	1	K2	CO3
10.	The primary characteristic of asynchronous sequential logiccircuits is a) They requiremultiple clock pulses for operation b) Their outputs depend onboth inputs and the order of input changes c) They depend only on clock signals d) They cannot store stateinformation	1	K1	CO4

11.	A asynchronous hazard is a		1	K1	CO4
	a) Logical hazard	b) Static hazard			
	c) Dynamic hazard	d) All ofthe above			
12.	In a stable asynchronous circuit, a transition table must:		1	K2	CO4
	a) Contain no don't-care conditions	b) Eliminate all redundant states			
	c) Map each state to a single next state for each input	d) Represent all possibleinput combinations			
13.	VHDL stand for:		1	K1	CO5
	a) Virtual Hardware Description Language	b) Very High-SpeedDigital Logic			
	c) Very High-Speed Integrated Circuit HardwareDescription Language	d) Variable High-Speed Device Language			
14.	In VHDL, the When statement is most commonly used for:		1	K1	CO5
	a) Loops	b) Conditional signal assignment			
	c) Generating clock signals	d) Defining state transitions			
15.	A reserved keyword in VHDL		1	K2	CO5
	a) Begin	b) Data			
	c) Flip	d) Counter			
16.	Output ports required for implementinga VHDL code for 3:8 encoder		1	K2	CO5
	a) 1	b) 3			
	c) 4	d) 5			

PART – A (ii) (Short Answer Questions)
(8 × 3 = 24 Marks)

Answer ALL Questions

17.	Demonstrate with an example Noise margin and propagation delay.	3	K2	CO1
18.	Convert the binary number 0110101110001100 to a hexadecimal number.	3	K3	CO1
19.	Outline two examples of combinational logic circuits.	3	K2	CO2
20.	Construct a demultiplexer circuit	3	K3	CO2
21.	Reproduce a T flip-flop using a JK flip-flop.	3	K2	CO3
22.	Identify the characteristics of asynchronous sequential circuits.	3	K3	CO4
23.	Identify the causes and effects of critical race conditions.	3	K3	CO4
24.	Choose and outline any two differences between different modeling styles of VHDL.	3	K3	CO5

PART - B (Descriptive Answer Questions)
(5 × 12 = 60 Marks)

Answer ALL Questions

25.	a)	Construct a TTL logic circuit for three input NAND gate and explain in detail.	12	K3	CO1
		OR			
	b)	Solve the following Boolean function for minimal SOP and POS form using K-Map. $F(A,B,C,D) = \Sigma(1,4,5,6,7,10,11,14)$	12	K3	CO1
26.	a)	Design a Binary to Gray code converter and implement the same using logic gates.	12	K3	CO2
		OR			
	b)	Design a 3 x 8 decoder using 2 x 4 decoders and explain its operation as a minterm generator.	12	K3	CO2

27.	a)	Make use of Master slave JK flipflop and explain the working of with necessary timing diagram.	*12*	*K3*	*CO3*
		OR			
	b)	Design and implement MOD-6 Ripple down counter using T flip flop.	*12*	*K3*	*CO3*
28.	a)	Make use of hazards and explain in detail about combinational circuits and sequential circuits with an example.	*12*	*K3*	*CO4*
		OR			
	b)	Construct the following using PLA.. W(A,B.C.D) = ∑m(2,12,13) X(A,B.C.D) = ∑m(7,8,9,10,11,12,13,14,15) Y(A,B.C.D) = ∑m(0,2,3,4,5,6,7,8,10,11,15) Z(A,B.C.D) = ∑m(1,2,8,12,13)	*12*	*K3*	*CO4*
29.	a)	Make use of VHDL and write a program for a behavioral model of a Full Adder.	*12*	*K3*	*CO5*
		OR			
	b)	Develop the behavioral and structural model of a Full Subtractor.	*12*	*K3*	*CO5*