Reg. No.												

Question Paper Code	12483

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023

Fourth Semester

Electronics and Instrumentation Engineering

20EIPW401 - DIGITAL ELECTRONICS WITH LABORATORY

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	State De-Morgan's law.	*2,K1,CO1*
2.	Define 'Minterm' and 'Maxterm'.	*2,K1,CO1*
3.	Design a half subtractor using logic gates.	*2,K2,CO2*
4.	What is meant by combinational circuits?	*2,K1,CO2*
5.	Compare Synchronous and Asynchronous circuits.	*2,K1,CO3*
6.	Draw a NAND based logic diagram of JK FF.	*2,K1,CO3*
7.	What is FPGA?	*2,K1,CO4*
8.	Define races.	*2,K1,CO4*
9.	Define Data flow model.	*2,K1,CO5*
10.	Write an entity declaration for 1x8 De-Mux.	*2,K1,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	Simplify the following Boolean function for minimal SOP and POS form using K-Map.	
		(i) $F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10) + \Sigma d(3,7)$	*6, K2,CO1*
		(ii) $F(A,B,C,D) = \Pi(1,3,5,7,12,13,14,15)$	*7, K2,CO1*
		OR	
	b)	(i) Design a TTL logic circuit for three input NAND gate.	*6, K2,CO1*
		(ii) Compare totem pole output with open collector output.	*7, K2,CO1*
12.	a)	Design a BCD to Excess 3 code converter and implement the same using logic gates.	*13, K3,CO2*
		OR	
	b)	Design and implement 3 to 8 line Decoder.	*13, K3,CO2*

13. a) A sequential circuit with 2 D-FFs A and B and two inputs X and Y, one output Z is specified by the following next state and output equations. *13, K3,CO3*

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA \quad ; \quad Z = B$$

(a) Draw the logic diagram of the circuit
(b) Derive the state tables
(c) Draw the state diagram.

OR

b) Explain in detail about the pulse- triggered S-R Flip Flop with necessary diagrams. *13, K2,CO3*

14. a) Explain the types of shift register in detail. *13, K2,CO4*

OR

b) Design the following using PLA and PROM. *13, K2,CO4*

$W(A,B.C.D) = \sum m(2,12,13)$
$X(A,B.C.D) = \sum m(7,8,9,10,11,12,13,14,15)$
$Y(A,B.C.D) = \sum m(0,2,3,4,5,6,7,8,10,11,15)$
$Z(A,B.C.D) = \sum m(1,2,8,12,13)$

15. a) Discuss in detail different modeling styles of VHDL with suitable example. *13, K2,CO5*

OR

b) Write the behavioral and structural model of a Full Adder using VHDL. *13, K3,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) (i) Derive the PLA programming table for the combinational circuit that squares a 3 bit number. *10,K3,CO4*

(ii) Build the VHDL code for 1x8 De-Mux. *5,K3,CO5*

OR

b) (i) Build the VHDL code for 4 bit Ripple counter. *10,K3,CO5*

(ii) Compare three combinational circuits PLA,PAL and ROM. *5,K2,CO4*