Reg. No.															

Question Paper Code	12824

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

Fourth Semester

Electronics and Instrumentation Engineering

(Common to Instrumentation and Control Engineering)

20EIPW401 – DIGITAL ELECTRONICS WITH LABORATORY

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.	2	K2	CO1
2.	List the important CMOS characteristics.	2	K1	CO1
3.	Mention the dependency of output in combinational circuits.	2	K2	CO2
4.	Give one application each for Multiplexer and Decoder.	2	K1	CO2
5.	Give the characteristic equation and characteristic table of a T- flip-flop.	2	K1	CO3
6.	Identify the number of flip-flop needed to realize mod-16 counter.	2	K2	CO3
7.	Differentiate synchronous and asynchronous sequential circuits.	2	K2	CO4
8.	Illustrate the concept of critical race. Why should it be avoided?	2	K2	CO4
9.	List the languages that are combined together to get VHDL language.	2	K1	CO5
10.	Give the HDL code for half adder.	2	K1	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Evaluate: $(ABCD.1234)_{16}$ $= (?)_8$	3	K3	CO1
		$= (?)_{10}$	3		
		$= (?)_2 = (?)_{BCD}$	4		
		$= (?)_5$	3		
		OR			
	b) i)	Simplify the following function using Karnaugh Map. $F(W,X,Y,Z) = \sum m(0,1,3,9,10,12,13,14) + \sum d(2,5,6,11)$.	7	K3	CO1
	ii)	Draw the MOS logic circuit for NOT gate and explain its operation.	6	K2	CO1
12.	a) i)	Design a full adder using 4x1 multiplexer, also write its truth table and draw the logical diagram.	7	K3	CO2
	ii)	Implement the following function using a suitable multiplexer f (a,b,c) $= \sum m(3,7,4,5)$	6	K3	CO2

OR

b) Design a combinational circuit with three inputs x, y, z and the three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is one less than the input. *13 K3 CO2*

13. a) Show the state transition diagram of a sequence detector circuit that detects '1010' from input data stream using Moore model. *13 K3 CO3*

OR

b) Design a sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12, 14 repeatedly. Use D flip-flops for your design. *13 K3 CO3*

14. a) Consider an asynchronous sequential circuit described by *K2 CO4*
$Y= x_1 x'_2 + (x_1 + x'_2) y$; Z=Y, where Y and Z are excitation and output functions respectively.
(i) Give the logic diagram of the circuit. *3*
(ii) Interpret the transition table and output map. *7*
(iii) Obtain its flow table. *3*

OR

b) Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions. *13 K2 CO4*
F1(A,B,C)= $\sum$ (0, 1, 2, 4)
F2(A,B,C)=$\sum$ (0, 5, 6, 7)

15. a) Describe the modeling techniques available in HDL. Give the VHDL code to realize a full adder using Behavioral modeling. *13 K2 CO5*

OR

b) Design a 8X1 multiplexer and write the VHDL code to realize it using structural & Behavioral modeling. *13 K2 CO5*

PART - C (1 × 15 = 15 Marks)

16. a) i) Plot the logical expression: ABCD + AB'C'D' + AB'C + AB on a 4 variable K-map; obtain the simplified expression from the map. *8 K3 CO1*
ii) Implement Full adder using suitable decoder. *7 K2 CO2*

OR

b) i) Express the function Y = A + B'C in canonical SOP and canonical POS form. *8 K3 CO1*
ii) Implement octal to binary encoder. *7 K2 CO2*