Reg. No.												

Question Paper Code	12531

B.E. / B.Tech. / M.Tech. - DEGREE EXAMINATIONS, NOV/DEC 2023

Second Semester

Information Technology

(Common to Computer Science and Engineering, Computer Science and Engineering (IoT), Computer Science and Engineering (Cyber Security) & M.Tech. - Computer Science and Engineering)

20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Regulations 2020)

Duration: 3 Hours Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks, K-Level, CO
1.	Prove the following using Demorgan's theorem [(X+Y)'+(X+Y)']'=X+Y	*2,K1,CO1*
2.	Represent XOR gate using only 4-NAND gates.	*2,K2,CO1*
3.	Define self-complementing code.	*2,K1,CO2*
4.	Trace the truth table for BCD to Excess-3 code converter.	*2,K2,CO2*
5.	Differentiate Mealy and Moor machines.	*2,K2,CO3*
6.	Give the characteristics table and equation of JK flipflop.	*2,K2,CO3*
7.	Define cycles and races.	*2,K1,CO4*
8.	Define Essential Hazard.	*2,K1,CO4*
9.	Describe about Shared Row method.	*2,K2,CO5*
10.	List any two drawbacks of asynchronous circuits.	*2,K2,CO5*

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

11.	a)	(i) Represent the Boolean function in SOP and POS Form. F(A,B,C,D)=∑m(0,1,2,5,8,9,10)	*7,K2,CO1*
		(ii) Plot the following Boolean function in k-map and simplify it. F(W,X,Y,Z)=∑m(0,1,2,4,5,6,8,9,12,13,14).	*6,K2,CO1*
		OR	
	b)	Indicate the Minimized expression using K-map method F=∑m(0,1,9,15,24,29,30) +∑d(8,11,31).	*13,K2,CO1*
12.	a)	Develop a code converter that converts a 8421 to BCD code.	*13,K3,CO2*
		OR	
	b)	Develop a logic circuit that accepts a 4bit Gray code and converts it into 4bit binary code.	*13,K3,CO2*

13. a) Develop a binary counter using JK flip flops to count in the following sequences: 000, 001, 010,011, 100, 101,111, 000. *13,K3,CO3*

OR

b) Develop T flipflop using D flipflop and JK flipflop using D flipflop. *13,K3,CO3*

14. a) Establish an asynchronous sequential circuit with 2 inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0; the output does not change for any change in X. Use SR latch for implementation of the circuit. *13,K3,CO4*

OR

b) Develop asynchronous sequential circuit which is described by the following excitation and output function *13,K3,CO4*

$Y=X_1X_2+(X_1+X_2)Y$, $Z=Y$.

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map and describe the behavior of the circuit.

15. a) (i) Explain the Race-free state assignment procedure. *7,K3,CO5*

(ii) Reduce the number of states in the following state diagram. Tabulated the reduced state table and Draw the reduced state diagram. *6,K3,CO5*

Present state	Next state		output
	x=0	x=1	x=0,x=1
A	A	B	0,0
B	C	D	0,0
C	A	D	0,0
D	E	F	0,1
E	A	F	0,1
F	G	F	0,1
G	A	F	0,1

OR

b) Develop a serial adder using a full adder and a flipflop. *13,K3,CO5*

PART - C (1 × 15 = 15 Marks)

16. a) Implement the switching functions. *15,K3,CO6*

Z1=ab'd'e+a'b'c'd'e'+bc+de;
Z2=a'c'e;Z3=bc+de+c'd'e'+bd;
Z4=a'c'e+ceusing 5 x8 x4PLA

OR

b) Implement the following function using PAL. *15,K3,CO6*

F1(A,B,C)=Σ(1,2,4,6);
F2(A,B,C)=Σ(0,1,6,7);
F3(A,B,C)=Σ(1,2,3,5, 7).