Reg. No.															

Question Paper Code	14182

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Second Semester

Computer Science and Engineering

(Common to Information Technology & Computer Science and Engineering (Cyber Security))

20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The complement of a sum is equal to the product of the complements is ---------- (a) Commutative Law (b) Distributive Law (c) Demorgan's Law (d) Consensus Law	1	K1	CO1
2.	Convert the octal number $(4356)_8$ to Decimal number. (a) $(2276)_{10}$ (b) $(2286)_{10}$ (c) $(2176)_{10}$ (d) $(2186)_{10}$	1	K2	CO1
3	If A and B are the inputs of a half adder, the sum is given by _____ (a) A EX-NOR B (b) A XOR B (c) A OR B (d) A AND B	1	K1	CO2
4.	Which one is not the outcome of magnitude comparator _____ (a) a < b (b) a = b (c) a > b (d) a – b	1	K1	CO2
5.	A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as? (a) Tristate (b) End around (c) Universal (d) Conversion	1	K1	CO3
6.	Placing an inverter between the inputs of S-R flip flop makes it a----flip flop (a) T (b) D (c) J-K (d) Master slave	1	K2	CO3
7.	Which of the following is NOT a Hardware Description Language (HDL)? (a) Verilog (b) VHDL (c) C++ (d) System Verilog	1	K1	CO4
8.	Which of the following HDLs is primarily used for designing digital circuits and systems? (a) Verilog (b) Python (c) C++ (d) Java	1	K1	CO4
9.	The race in which stable state depends on order is called (a) Critical race (b) Identical race (c) Non critical race (d) Defined race	1	K1	CO5
10.	EPROM can be (a) UVPROM (b) EEPROM (c) both a and b (d) None of the above	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Explain "Maxterm" and "Minterm".	2	K2	CO1
12.	State DeMorgan's theorem and mention its use.	2	K1	CO1
13.	Explain Combinational logic circuit.	2	K2	CO2
14.	Define Priority Encoder.	2	K1	CO2
15.	Difference between Latch and Flip Flop.	2	K2	CO3
16.	State the excitation table of JK Flip Flop.	2	K1	CO3
17.	Discuss the data flow modelling of a 4-bit comparator.	2	K2	CO4
18.	What is the purpose of process block in VHDL?	2	K1	CO4
19.	Differentiate races and cycles.	2	K2	CO5
20.	Define critical race.	2	K1	CO5
21.	Define Static RAM and Dynamic RAM.	2	K1	CO6
22.	Define memory decoding.	2	K1	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Explain the Minimal Sum of Products form of the Switching function F(a,b,c,d)=Σm(0,2,4,6,8)+Σd(10,11,12,13,14,15).	11	K2	CO1
		OR			
	b)	Illustrate the following Boolean function after reducing it with logic gates. F (A, B, C, D) = ∑m (1, 3, 4, 11, 12, 13, 14, 15).	11	K2	CO1
24.	a)	Explain the functions and need of encoder and decoder.	11	K2	CO2
		OR			
	b)	Explain the construction a 16:1 multiplexer using a 4:1 multiplexer.	11	K2	CO2
25.	a)	Explain the 4-bit SISO, and PIPO shift register with its waveforms.	11	K2	CO3
		OR			
	b)	Explain the design of Synchronous MOD -6 counter.	11	K2	CO3
26.	a)	Design a 2-to-1 multiplexer (MUX) using Verilog.	11	K3	CO4
		OR			
	b)	Draw a full adder circuit and write a code using Verilog HDL.	11	K3	CO4
27	a)	Design a race free circuit and also explain about races and methods to eliminate races.	11	K3	CO5
		OR			
	b)	Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes '1', the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.	11	K3	CO5
28.	a)	Explain the implementation of the following function using PAL. X (A, B, C,D) = Σm(0,2,6,7,8,9,12,13,14); Y (A, B,C,D) = Σm(2,3,8,9,10,12,13).	11	K2	CO6
		OR			
	b)	Discuss in detail about various types of ROM.	11	K2	CO6