Question Paper Code	12654

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024
Second Semester
Information Technology
(Common to Computer Science and Engineering, Computer and Communication and Cyber Security)
20ESIT203 - DIGITAL PRINCIPLES AND SYSTEM DESIGN
Regulations - 2020

Duration: 3 Hours   Max. Marks: 100

PART - A (10 × 2 = 20 Marks)
Answer ALL Questions

		Marks	K-Level	CO
1.	Convert Y=A+BC'+AB+A'BC into canonical form.	2	K2	CO1
2.	Convert a given binary number 110111 into a decimal number system.	2	K2	CO1
3.	Draw the logic diagram of a 3 bit adder.	2	K1	CO2
4.	Define priority encoder.	2	K1	CO2
5.	Draw the state diagram of 3 bit Up/ Down Synchronous Counter.	2	K1	CO3
6.	Differentiate synchronous and asynchronous circuits.	2	K2	CO3
7.	Differentiate between cycles and races.	2	K2	CO5
8.	Define Hazards and mention its types.	2	K1	CO5
9.	Differentiate between EEPROM and PROM.	2	K2	CO6
10.	Define memory decoding.	2	K1	CO6

PART - B (5 × 13 = 65 Marks)
Answer ALL Questions

			Marks	K-Level	CO
11.	a)	Find the Minimal Sum of Products representation for $F(A,B,C,D,E) = \sum m(1,4,6,10,20,22,24,26) + \sum d(0,11,16,27)$ using K-Map method.	13	K2	CO1

OR

			Marks	K-Level	CO
	b)	State and prove the the following in Boolean Algebra i. Commutative Law ii. Associative law iii. Distributive Law iv. DeMorgan's Theorem v. Absorption Theorem	13	K2	CO1

			Marks	K-Level	CO
12.	a)	Illustrate a 4-bit magnitude comparator with three outputs : A<B, A=B, A>B.	13	K2	CO2

OR

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create   **12654**

b) i) Illustrate 4 x 16 decoder using two 3 x 8 decoders with enable input. *7* *K2* *CO2*

ii) Find the following functions using a multiplexer. $F(W,X,Y,Z)= \sum m$ (0,1,3,4,8,9,15). *6* *K2* *CO2*

13. a) Illustrate with diagram the logic circuit of SR Flip-flop using D flip-flop and T flip-flop. *13* *K2* *CO3*

OR

b) Explain in detail about the following registers: *13* *K2* *CO3*
(a)Serial in Serial out register.
(b)Serial in Parallel out register.

14. a) Give hazard-free realization for the following boolean function. *13* *K2* *CO5*
(a) $F(I,J,K,L)= \sum (1,3,4,5,6,7,9,11,15)$
(b) $F(W,X,Y,Z)=\sum(0,2,3,4,6,7,8,9,11,13)$

OR

b) Design an asynchronous sequential circuit that has 2 inputs x2 and x1 and 1 output z, when x1=0 the output z is 0 the first change in x2 that occurs while x1 is 1 will cause output z to be 1 the output z will remain 1 until x1 returns to zero. *13* *K2* *CO5*

15. a) Implement the following function using PAL. *13* *K2* *CO6*
F1 (A, B,C) = Σ(1, 2, 4, 6);
F2 (A, B, C) = Σ(0, 1, 6, 7);
F3 (A, B,C) = Σ(1, 2, 3, 5, 7).

OR

b) i) A combinational circuit is defined by the functions: $F1=\sum m(3,5,7)$ $F2=\sum m(4,5,7)$ implement the circuit with PLA having 3 inputs, 3 product terms and two outputs. *6* *K2* *CO6*

ii) Draw the PLA circuit to implement the logic functions A'BC+AB'C+AC' and A'B'C'+BC. *7* *K2* *CO6*

PART - C (1× 15 = 15 Marks)

16. a) Demonstrate the characteristics of T flip-flop and SR flip-flop using the Verilog HDL. *15* *K2* *CO4*

OR

b) Discuss about $n:2^n$ Decoder with dataflow modelling with the n value is 3 and write a program using Verilog HDL. *15* *K2* *CO4*