B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2023
Third Semester
Information Technology
(Common to Computer Science and Engineering, Computer and Communication
Engineering & M.Tech. - Computer Science and Engineering(Integrated))
20ITPC303 - COMPUTER ORGANIZATION AND ARCHITECTURE
(Regulations 2020)

Duration: 3 Hours   Max. Marks: 100

PART - A (10 × 2 = 20 Marks)
Answer ALL Questions

		Marks, K-Level, CO
1.	What is instruction register?	2,K1,CO1
2.	How CPU execution time for a program is calculated?	2,K1,CO1
3.	Find the value of 100011 * 100010.	2,K1,CO2
4.	Outline the IEEE standard floating -point formats.	2,K1,CO2
5.	What is a data path element?	2,K1,CO3
6.	Show the 5 stages of pipelining.	2,K1,CO3
7.	What is data level parallelism?	2,K1,CO4
8.	Compare SMT and hardware multithreading.	2,K2,CO4
9.	What is message passing?	2,K1,CO6
10.	List the benefits of clustering in computer architecture.	2,K1,CO6

PART - B (5 × 13 = 65 Marks)
Answer ALL Questions

11. a) Computer A runs a program in 12 seconds with 3 GHz clock. We have to design a computer B such that it can run the same program within 9 seconds. Determine the clock rate for computer B. Assume that due to an increase in clock cycle rate, CPU design of computer B is affected and it requires 1.2 times as many clock cycles as computer A for execution of this program.   *13,K2,CO1*

OR

   b) Explain the various MIPS addressing modes with suitable examples.   *13,K2,CO1*

12. a) (i) Multiply the following pair of signed 2's complement numbers using Booth's algorithm, A= $(-13)_{10}$ = $(110011)_2$ and B= $(-20)_{10}$ = $(101100)_2$ where A is multiplicand and B is multiplier.   *7,K2,CO2*

(ii) Multiply the following numbers using bit pair recoding *6,K2,CO2*
A=01111   multiplicand (15) and
B= 10110   multiplier   (-10)

OR

b) Discuss in detail the sequential version of the multiplication algorithm and hardware with a neat diagram. *13,K2,CO2*

13. a) Explain data hazards and how to overcome it. *13,K2,CO3*

OR

b) Summarize R-Type instructions and explain the functional block diagram with control signals for basic implementation of MIPS subset. *13,K2,CO3*

14. a) Explain clusters in detail with neat diagram. *13,K2,CO4*

OR

b) Describe the types of multithreading and its advantages *13,K2,CO4*

15. a) Explain DMA in detail with neat diagram. *13,K2,CO6*

OR

b) Discuss the methods used to measure and improve the performance of the cache. *13,K2,CO6*

PART - C (1 × 15 = 15 Marks)

16. a) Describe the working of warehouse scale computers in detail. *15,K2,CO5*

OR

b) Explain the classification of shared memory multiprocessor based on memory access latency. *15,K2,CO5*