Reg. No.															

Question Paper Code	13291

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2024

Third Semester

Information Technology

(Common to Computer Science and Engineering, M.Tech - Computer Science and Engineering (5 years Integrated) & Computer and Communication Engineering)

20ITPC303 - COMPUTER ORGANIZATION AND ARCHITECTURE

Regulations - 2020

Duration: 3 Hours Max. Marks: 100

PART - A (MCQ) (20 × 1 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	What addressing mode involves using an index register to access elements of an array? (a) Base-register addressing (b) Indexing (c) Displacement addressing (d) Relative addressing	1	K1	CO1
2.	The utility program employed to load the object code into memory for execution is called (a) loader (b) fetcher (c) extractor (d) linker	1	K1	CO1
3.	What is the characteristic of a random-access memory (RAM)? (a) It is inexpensive and permanent (b) It has a long access time (c) Any location can be accessed in a short and fixed amount of time (d) It retains data when power is turned off	1	K1	CO1
4.	When dividing 0.75 by 0.25 using decimal arithmetic, what is the result? (a) 3 (b) 0.3 (c) 30 (d) 7.5	1	K1	CO2
5.	In floating-point multiplication, what is the exponent of the result? (a) The sum of the exponents of the operands (b) The difference between the exponents of the operands (c) The average of the exponents of the operands (d) The product of the exponents of the operands	1	K1	CO2
6.	What is the main challenge in floating-point subtraction when the exponents differ significantly? (a) Loss of precision (b) Overflow (c) Underflow (d) Exponentiation	1	K1	CO2
7.	Which type of MIPS instruction is used to perform arithmetic operations between registers? (a) I-type (b) J-type (c) R-type (d) S-type	1	K1	CO3
8.	What is the purpose of the Write Back (WB) stage in the MIPS datapath? (a) Fetch instructions from memory (b) Decode the instruction and read registers (c) Execute the instruction and perform arithmetic operations (d) Write the result of the computation back to the register file	1	K1	CO3
9.	Which of the following is a common technique to mitigate control hazards? (a) Register Renaming (b) Branch Prediction (c) Data Forwarding (d) Load Balancing	1	K1	CO3
10.	Which type of applications may not require shared addressing to run well on parallel hardware, according to the topic? (a) High-performance computing (b) Web search (c) Mail servers (d) Cache coherence	1	K1	CO4
11.	State whether the following statement is true or false: Warehouse-Scale Computers (WSC) are often classified as just large clusters. (a) True (b) False	1	K1	CO4

12. What major economic opportunity of scale led to the development of cloud computing? *1 K1 CO4*
    (a) Reduced operational costs
    (b) Enhanced server reliability
    (c) Increased cooling efficiency
    (d) Lower per-unit costs of Warehouse-Scale Computers (WSCs)
13. What is synchronization in the context of processors operating in parallel? *1 K1 CO5*
    (a) A process to acquire physical addresses (b) Coordination of shared data access
    (c) Fast memory access (d) Locking shared variables
14. What is a cluster in the context of parallel computing? *1 K1 CO5*
    (a) A network of computers functioning as a single large multiprocessor over a local area network
    (b) A cluster of servers with separate memory but interconnected cores
    (c) A shared-memory multiprocessor system
    (d) A group of interconnected microprocessors within a single server
15. What is the primary method of communication in message-passing multiprocessors? *1 K1 CO5*
    (a) Shared memory (b) Task-level parallelism
    (c) Explicit message passing (d) Cache coherence
16. What major economic opportunity of scale led to the development of cloud computing? *1 K1 CO5*
    (a) Lower per-unit costs of Warehouse-Scale Computers (WSCs)
    (b) Reduced operational costs
    (c) Enhanced server reliability
    (d) Increased cooling efficiency
17. Which component represents the slowest but most cost-effective storage in the computer's memory hierarchy? *1 K1 CO6*
    (a) Processor registers (b) Main memory
    (c) Level 2 (L2) cache (d) Magnetic disk
18. What memory technology is responsible for storing and transmitting data from external storage devices to the CPU and main memory? *1 K1 CO6*
    (a) Memory controller (b) Register memory
    (c) Random-Access Memory (RAM) (d) Cache memory
19. What is the role of cache management policies like Least Recently Used (LRU) in cache memory? *1 K1 CO6*
    (a) To determine the size of the cache
    (b) To decide which data to place in the cache and when to replace it
    (c) To control the power consumption of the cache
    (d) To establish the communication between CPU and cache
20. What does TLB contains? *1 K1 CO6*
    (a) Pages (b)Space (c) ROM (d) Page table

PART - B (10 × 2 = 20 Marks)

Answer ALL Questions

21. Write the components of a computer system and list their functions. *2 K1 CO1*
22. What is processor time? *2 K1 CO1*
23. Perform the binary addition of 1100 and 1010 and indicate if there is an overflow. *2 K2 CO2*
24. Write the basic steps involved in the restoring division algorithm. *2 K2 CO2*
25. Classify the different types of hazards with examples. *2 K2 CO3*
26. Differentiate static and dynamic prediction. *2 K2 CO3*
27. Differentiate strong scaling and weak scaling. *2 K2 CO4*
28. What is hardware multithreading? *2 K1 CO4*
29. Name the interconnections used in multiprocessor system. *2 K1 CO5*
30. What is the primary advantage of using GPUs for machine learning tasks? *2 K1 CO5*

PART - C (6 × 10 = 60 Marks)

Answer ALL Questions

31.	a)	Discuss in elaborately about the concept of MIPS addressing modes with examples.	*10*	*K2*	*CO1*
		OR			
	b)	Explain various Instruction formats and illustrate the same with an example.	*10*	*K2*	*CO1*
32.	a)	Interpret the result of subtracting numbers $(28)_{10}$ and $(15)_{10}$ using 6 bit 2's complement representation.	*10*	*K2*	*CO2*
		OR			
	b)	Describe in detail about the Booth algorithm with an example.	*10*	*K2*	*CO2*
33.	a)	Briefly discuss the basic concepts of pipelining with suitable example.	*10*	*K2*	*CO3*
		OR			
	b)	What are R-Type instructions? Draw and explain the functional block diagram with control signals for basic implementation of MIPS subset.	*10*	*K2*	*CO3*
34.	a)	Describe the main characteristics and limitations of instruction level parallelism.	*10*	*K2*	*CO4*
		OR			
	b)	Explain in detail about hardware multithreading in parallel processing.	*10*	*K2*	*CO4*
35.	a)	Explain how Graphics processing units helps to improve processor performance.	*10*	*K2*	*CO5*
		OR			
	b)	Discuss the challenges encountered in implementing parallel processing.	*10*	*K2*	*CO5*
36.	a)	Write brief notes on the various mapping schemes used in memory.	*10*	*K2*	*CO6*
		OR			
	b)	Write short notes on Direct Memory Access and Interrupts.	*10*	*K2*	*CO6*