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Question Paper Code	14001
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M.Tech / B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Information Technology

(Common to Computer Science and Engineering, Computer and Communication & M.Tech - Computer Science and Engineering)

20ITPC303 - COMPUTER ORGANIZATION AND ARCHITECTURE

Regulations - 2020

Duration: 3 Hours

Max. Marks: 100

**PART - A (MCQ) (10 × 1 = 10 Marks)**

Answer ALL Questions

	<i>Marks</i>	<i>K- Level</i>	<i>CO</i>
1. Which functional unit stores data and instructions before and after processing? (a) ALU (b) Memory Unit (c) Control Unit (d) Register	1	K2	CO1
2. Which of the following MIPS instructions uses PC-relative addressing? (a) lw (b) sw (c) beq (d) addi	1	K1	CO1
3. In processors, multiplication of two numbers is usually implemented using: (a) Repeated addition (b) Division algorithm (c) Shift and add method (d) Subtraction loops	1	K1	CO2
4. What is the result of the MIPS instruction sub \$s0, \$s1, \$s2? (a) \$s0 gets \$s1 + \$s2 (b) \$s0 gets \$s2 - \$s1 (c) \$s0 gets \$s1 - \$s2 (d) \$s1 gets \$s0 - \$s2	1	K1	CO2
5. In binary arithmetic, what is the result of 1 + 1? (a) 1 (b) 10 (c) 11 (d) 0	1	K2	CO3
6. What is the purpose of the carry flag in the processor status register? (a) Indicates division by zero (b) Indicates overflow in signed arithmetic (c) Indicates a carry out of the most significant bit (d) Indicates memory overflow	1	K1	CO3
7. A WAR (Write After Read) hazard can be eliminated by (a) Increasing clock speed (b) Adding more memory (c) Using out-of-order execution (d) Instruction pipelining	1	K1	CO4
8. In which type of hazard do multiple instructions try to use the same pipeline stage simultaneously? (a) Structural hazard (b) Data hazard (c) Control hazard (d) Load hazard	1	K2	CO4
9. In Flynn's taxonomy, SIMD is defined as (a) Single Instruction, Multiple Data (b) Sequential Instruction, Multiple Data (c) Simultaneous Instruction, Multiple Devices (d) Shared Instruction, Multi-Device	1	K1	CO5
10. During a DMA operation, the CPU is (a) Completely involved (b) Partially involved (c) Not involved in the data transfer (d) Required to initiate every byte transfer	1	K1	CO6

**PART - B (12 × 2 = 24 Marks)**

Answer ALL Questions

11. Name any two functional units of a CPU and state their functions.	2	K1	CO1
12. What is register addressing mode in MIPS?	2	K1	CO1
13. Find the bit pair code for multiplier 11010.	2	K2	CO2
14. Why is subword parallelism used in processors?	2	K2	CO2
15. How can data hazards be minimized in pipelined processors?	2	K2	CO3
16. Define pipeline speedup.	2	K1	CO3
17. List the five stages of instruction execution in a basic MIPS pipeline.	2	K1	CO4

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|---|---|----|-----|
| 18. What is SIMD in Flynn's classification?           | 2 | K1 | CO4 |
| 19. Define cache hit and cache miss.                  | 2 | K1 | CO5 |
| 20. Give one real-world example of an SIMD system.    | 2 | K1 | CO5 |
| 21. What is temporal locality in cache memory?        | 2 | K1 | CO6 |
| 22. How does DMA improve the performance of a system? | 2 | K2 | CO6 |

**PART - C (6 × 11 = 66 Marks)**

Answer ALL Questions

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| 23. a) Explain the core operational concepts of the memory management and data representation.   | 11 | K2 | CO1 |
| <b>OR</b>  |    |    |     |
| b) Summarize about decision making and explain how it is applied in MIPS.  | 11 | K2 | CO1 |
| 24. a) Apply the restoring division algorithm for the following numbers to perform division. Dividend = 1010, Divisor = 0011.                              | 11 | K3 | CO2 |
| <b>OR</b>  |    |    |     |
| b) Multiply the following pair of signed numbers using Booth's bit-pair recording of the multiplier. A = +13 (Multiplicand) and B = - 6 (Multiplier).      | 11 | K3 | CO2 |
| 25. a) Explain how floating point addition is carried out in a computer system? Give an example for a binary floating point addition.                      | 11 | K2 | CO3 |
| <b>OR</b>  |    |    |     |
| b) Discuss about different memory address layouts and brief about the techniques used to increase the average rate of fetching words from the main memory. | 11 | K2 | CO3 |
| 26. a) Explain how the instruction pipeline works? What are the various situations where an instruction pipeline can occur? Explain it with an example.    | 11 | K2 | CO4 |
| <b>OR</b>  |    |    |     |
| b) Discuss the limitation in implementing the processor path. Suggest the methods to overcome them.  | 11 | K2 | CO4 |
| 27. a) Explain the concept of Flynn's classification in detail.  | 11 | K2 | CO5 |
| <b>OR</b>  |    |    |     |
| b) Discuss the key characteristics of multi-core processors in detail.   | 11 | K2 | CO5 |
| 28. a) Illustrate the different types of DMA transfer modes, how they function, and their advantages over traditional data transfer methods.               | 11 | K2 | CO6 |
| <b>OR</b>  |    |    |     |
| b) Explain the concept of virtual memory with neat diagram and its significance.   | 11 | K2 | CO6 |