

PART - B ($5 \times 13 = 65$ Marks)

Answer ALL Questions

11. a) Explain the various MIPS instruction formats and illustrate the same ¹³ K² CO1 with an example.

OR

- b) i) Translate C code to MIPS assembly code f = (g + h) (i + j), the 5 K2 CO1 variables f, g, h, i and j are assigned to the registers \$s0,\$s1, \$s2, \$s3 and \$s4, respectively.
 - - 3) Addi \$s0, (\$s0), #1500 4) Move 16(R5), R3

- 12. a) i) Perform X + Y and X Y using 2'complement for the given two $6 K^2 CO^2$ binary numbers X = 0000 1010 1001 0111 and Y = 1110 1001 1010 1100.
 - ii) Perform the Booth's operation for the 5-bit signed operand, +23 is the 7 K2 CO2 multiplicand, and it's multiplied by -10, the multiplier to get the 10-bit product -230.

OR

- b) i) Briefly explain about the subword parallelism. 6 K2 CO2
 - ii) Add the numbers $(0.75)_{10}$ and $(-0.4375)_{10}$ in binary using the floating 7 K2 CO2 point addition algorithm.
- 13. a) With neat sketch explain the basic MIPS implementation with ¹³ K2 CO3 necessary multiplexers and control lines.

OR

- b) Explain the different types of pipeline hazards with suitable examples. ¹³ K2 CO3
- 14. a) Elaborate on Flynn's classification of parallel hardware with necessary ¹³ K2 CO4 examples.

OR

- b) Describe the four principle approaches of multithreading with ¹³ K2 CO4 necessary diagrams.
- 15. a) Outline the need for cache memory and list the three mapping methods ¹³ K² CO5 of cache memory and explain any two.

OR

b) Explain the virtual memory address translations in detail with ¹³ K2 CO5 necessary diagrams.

PART - C $(1 \times 15 = 15 \text{ Marks})$

- 16. a) A block set associative cache consists of a total of 64 blocks divided ¹⁵ K3 CO6 into four block sets. The main memory contains 4096 blocks, each consisting of 128 words.
 - a) How many bits are there in a main memory address?
 - b) How many bits are there in each of the TAG, SET and WORD fields?
 - c) What is the size of cache memory?

OR

b) Discuss the various memory mapping schemes. 15 K2 CO6

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