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Question Paper Code	12694
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M.E. / M.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

First Semester

M.E - Computer Science and Engineering

(Common to Computer Science and Engineering (with Specialization with Networks))

20PCNPC101 - ADVANCED COMPUTER ARCHITECTURE

Regulations - 2020

Duration: 3 Hours

Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

- | | Marks | K-
Level | CO |
|--|-------|-------------|-----|
| 1. Define Amdhal's Law. | 2 | K1 | CO1 |
| 2. Define dependency and list its types. | 2 | K1 | CO1 |
| 3. What do you mean by multiple Issue processors? | 2 | K1 | CO2 |
| 4. How to Enhance Dependability in Memory Systems. | 2 | K2 | CO2 |
| 5. Describe interconnection network. | 2 | K2 | CO3 |
| 6. Differentiate Buses from crossbar networks. | 2 | K2 | CO3 |
| 7. Explain warehouse. | 2 | K1 | CO4 |
| 8. Differentiate between SMT and CMP. | 2 | K2 | CO4 |
| 9. Differentiate between scalar and vector processors. | 2 | K2 | CO5 |
| 10. Describe the Vector functional units. | 2 | K2 | CO5 |

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

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|--|----|----|-----|
| 11. a) Discuss about Dynamic scheduling using Tomasulo's approach. | 13 | K2 | CO1 |
| OR | | | |
| b) Discuss how to reduce Branch cost with dynamic hardware prediction technique. | 13 | K2 | CO1 |
| 12. a) Explain the architecture and function of super scalar processor. | 13 | K2 | CO2 |
| OR | | | |
| b) Describe the various cache hit time reduction techniques for improving the cache performance. | 13 | K2 | CO2 |
| 13. a) Explain Centralized Shared Memory Architectures. | 13 | K2 | CO3 |

OR

K1 – Remember; K2 – Understand; K3 – Apply; K4 – Analyze; K5 – Evaluate; K6 – Create

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- b) i) Demonstrate the Cache Coherence Performance issues. 7 K2 CO3
 ii) Illustrate in detail Snooping Coherence Protocols. 6 K2 CO3
14. a) Explain the SUN CMP architecture in detail and Analyze Intel Multicore Architecture. 13 K2 CO4

OR

- b) i) Explain Google Warehouse-Scale Computer 7 K2 CO4
 ii) Explain the customized and standardize IAAA container for Google. 6 K2 CO4
15. a) i) Describe Vector Architecture in detail. 7 K2 CO5
 ii) Explain the details of handling Multidimensional Arrays in Vector Architectures 6 K2 CO6

OR

- b) i) Identify the need for SIMD Extension for multimedia. 7 K2 CO5
 ii) Explain how to Handle Sparse Matrices in Vector Architectures. 6 K2 CO6

PART - C (1 × 15 = 15 Marks)

16. a) Prepare the primary components of the instruction set architecture of VMIPS and explain the basic vector architecture with neat block diagram. 15 K3 CO6

OR

- b) Order the issues in Eliminating Dependent Computations and Finding Dependences. 15 K3 CO6