Reg. No.												

Question Paper Code	12695

M.E. / M.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2024

First Semester

M.E - Embedded Systems Technologies

20PESPC101 - ADVANCED DIGITAL PRINCIPLES AND DESIGN

Regulations - 2020

Duration: 3 Hours | Max. Marks: 100

PART - A (10 × 2 = 20 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Distinguish Synchronous and Asynchronous sequential circuits.	2	K2	CO1
2.	Enumerate the elements present in ASM chart.	2	K2	CO1
3.	What do you meant by race around condition?	2	K1	CO2
4.	What is an essential hazard?	2	K2	CO2
5.	How is Fault Simulation used in testing?	2	K1	CO3
6.	Define defect, error and fault.	2	K2	CO3
7.	List the features of FPGA.	2	K1	CO4
8.	What is EPLD?	2	K2	CO4
9.	Write the structure of the entity in VHDL.	2	K1	CO5
10.	Mention any two operators used in VHDL.	2	K2	CO5

PART - B (5 × 13 = 65 Marks)

Answer ALL Questions

			Marks	K – Level	CO
11.	a)	Describe State table assignment and reduction of clocked synchronous sequential circuits with an example.	13	K2	CO1
		OR			
	b)	Draw the ASM chart for binary multiplier.	13	K2	CO1
12.	a)	Design an Asynchronous sequential circuit with input A and B and an output Y. Initially at any time if both the inputs are 0, the output, Y=0. When A or B = 1, Y =1. When the other input also become 1, Y=0. The output stays at 0 until circuit goes back to initial state.	13	K3	CO2
		OR			
	b)	Illustrate about different hazards that occur in sequential circuits and also about the way to eliminate them.	13	K2	CO2

13. a) Describe any one path sensitization method of ATPGs with a suitable example. *13 K2 CO3*

OR

b) Generate the test vector and signature analysis for the circuit under test using BIST algorithm. *13 K2 CO3*

14. a) Explain about the structure of Xilinx 2000 CLB and IO units with neat diagram. *13 K2 CO4*

OR

b) Using PALs, determine the circuit used to realize the following Boolean functions. *13 K2 CO4*
(i) W(A,B,C,D) = ∑ (0,2, 6,7,8,9,12,13)
(ii) X(A,B,C,D) = ∑ (0, 2, 6, 7, 8, 9, 12, 13, 14)
(iii)Y(A, B, C, D) = ∑ (2, 3, 8, 9, 10, 12, 13)

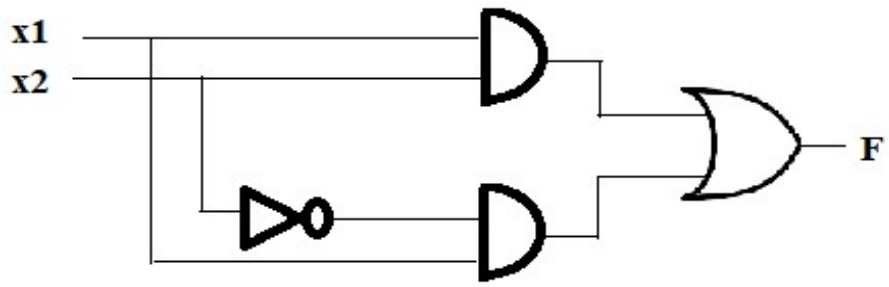
15. a) What is Gate level modelling? Explain with a suitable example. *13 K2 CO5*

OR

b) Write a VHDL program for 4:1 multiplexer. *13 K2 CO5*

PART - C (1 × 15 = 15 Marks)

16. a) For the circuit shown below, obtain the Boolean difference with respect to x2. *15 K3 CO3*



OR

b) Describe about ripple carry adder and model it with VHDL code. *15 K3 CO5*