Reg. No.																

Question Paper Code	13975

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Computer and Communication Engineering

24COPC301 - DIGITAL DESIGN AND COMPUTER ORGANIZATION

Regulations - 2024

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The octal equivalent of binary 110110 is: a) 56 b) 66 c) 64 d) 76	1	K1	CO1
2.	A logic gate that implements Y = A′B + AB′ is: a) XOR b) XNOR c) NAND d) NOR	1	K1	CO1
3.	The sum output of a half adder is obtained using: a) XOR gate b) AND gate c) OR gate d) NOR gate	1	K1	CO2
4.	In BCD code, each decimal digit is represented by: a) 4 bits b) 8 bits c) 2 bits d) 10 bits	1	K1	CO2
5.	A flip-flop that toggles its state on each clock pulse is: a) D flip-flop b) SR flip-flop c) T flip-flop d) None	1	K1	CO3
6.	The basic building block of a sequential circuit is: a) Logic gate b) Flip-flop c) Register d) Counter	1	K1	CO3
7.	The part of instruction that specifies the operation to be performed is: a) Operand b) Opcode c) Address field d) Register field	1	K1	CO4
8.	The memory used in micro programmed control is called: a) Control Memory (CM) b) Main Memory c) Cache d) ROM	1	K1	CO4
9.	The fastest memory in a computer system is a) Cache b) Main memory c) Registers d) Hard disk	1	K1	CO5
10.	A pipeline is divided into a series of: a)Buffers b)Registers c) Stages d) Blocks	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Find the octal equivalent of hexadecimal numbers of AB.CD.	2	K2	CO1
12.	Illustrate NOR Operation with a truth table.	2	K2	CO1
13.	List the truth table of full subtractor.	2	K1	CO2
14.	Differentiate between encoder and decoder.	2	K2	CO2
15.	Summarize the characteristic table and equation of JK flip flop.	2	K2	CO3
16.	Difference between the performance of asynchronous and synchronous counter.	2	K2	CO3
17.	List the functional units of digital computer.	2	K1	CO4
18.	Outline the instruction cycle with a diagram.	2	K2	CO4
19.	What is the purpose of cache memory?	2	K1	CO5
20.	What is programmed I/O?	2	K1	CO5
21.	Define pipelining.	2	K1	CO6
22.	What is parallelism?	2	K1	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Present the graphical symbol, algebraic expression and truth table for the following digital logic gates: AND, OR, Inverter, Buffer, NAND, NOR, Exclusive OR and Exclusive NOR.	*11*	*K3*	*CO1*
		OR			
	b)	Minimize the following function using Karnaugh map F(A,B,C,D) = ∑m(0,1,2,3,4,5,6,11,12,13) and implement with logic gates.	*11*	*K3*	*CO1*
24.	a)	Explain the full adder with inputs x,y,z and two outputs S and C. The circuits perform x+y+z is the input carry, C is the output carry and S is the Sum & realize it's using only NOR gates.	*11*	*K2*	*CO2*
		OR			
	b)	Describe the procedure of converting 8421 to Gray code converter also realize the converter using only NAND gates.	*11*	*K2*	*CO2*
25.	a)	Explain T flip-flop using D flip-flop and JK using D flip flop.	*11*	*K2*	*CO3*
		OR			
	b)	Explain the different types of shift registers with neat diagram.	*11*	*K2*	*CO3*
26.	a)	What is an addressing mode? Outline the types of addressing mode with an example.	*11*	*K2*	*CO4*
		OR			
	b)	Discuss the concept of control signals and their role in CPU operation.	*11*	*K2*	*CO4*
27.	a)	Discuss how memory mapping techniques are useful for finding the memory blocks in cache.	*11*	*K2*	*CO5*
		OR			
	b)	Explain the working principle of DMA with neat diagram.	*11*	*K2*	*CO5*
28.	a)	Describe data hazards and control hazards. Explain with suitable techniques, how these hazards can be mitigated.	*11*	*K2*	*CO6*
		OR			
	b)	Explain Instruction-Level Parallelism (ILP) and techniques to achieve it.	*11*	*K2*	*CO6*