

B.E. / B.Tech. / M.Tech.- DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Computer Science and Engineering

(Common to Information Technology & M.Tech. - Computer Science and Engineering)

24CSPW301 - DIGITAL DESIGN AND COMPUTER ORGANIZATION WITH LABORATORY

Regulations - 2024

Duration: 3 Hours

Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

	Marks	K- Level	CO
1. Which of the following represents the basic building blocks of a digital logic circuit? (a) Diodes (b) Transistors (c) Resistors (d) Capacitors	1	K1	CO1
2. Which binary code is also known as the "8421 code"? (a) Gray code (b) Excess-3 code (c) BCD (d) Two's complement code	1	K1	CO1
3. What does the term "combinational logic" mean in digital electronics? (a) A type of logic gate (b) Logic circuits with no feedback loops (c) A type of flip-flop (d) A type of memory unit	1	K1	CO2
4. What is the output of an XOR gate when both of its inputs are set to 1? (a) 0 (b) 1 (c) Undefined (d) Depends on other factors	1	K1	CO2
5. A latch is _____ sensitive (a) Level (b) Edge (c) Both Level and Edge (d) None of the mentioned	1	K1	CO3
6. T Flip flop is used as (a) Transfer data circuit (b) Time delay switch (c) Toggle switch (d) None of the mentioned	1	K1	CO3
7. Which of the following best describes the role of a guard bit in rounding operations? (a) It increases the exponent range (b) It reduces the overall computation time (c) It acts as an additional digit to improve rounding accuracy (d) It minimizes memory usage	1	K1	CO4
8. The normalized representation of $0.0010110 * 2^9$ is _____ (a) $1.11010 * 2^3$ (b) $1.0110 * 2^6$ (c) $1.0110 * 2^{12}$ (d) $1.0110 * 2^9$	1	K1	CO4
9. Which of the following is a drawback of message-passing multiprocessors? (a) Simplicity in programming (b) Scalability (c) Isolation of failures (d) High communication overhead	1	K1	CO5
10. Which of the following is the fastest means of memory access for CPU? (a) Cache (b) Registers (c) Main memory (d) Virtual memory	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11. Given the two binary numbers $X = 1010100$ and $Y = 1000011$, show the subtraction using 2's complements. (a) $X - Y$ and (b) $Y - X$.	2	K2	CO1
12. Translate the following Boolean expression with a minimum number of literals. $F = (BC' + A'D)(AB' + CD')$.	2	K2	CO1
13. Demonstrate the 2 bit subtractor.	2	K2	CO2
14. Infer a 1 bit magnitude comparator with a logic diagram.	2	K2	CO2
15. Compare synchronous and asynchronous counters.	2	K2	CO3
16. List the types of Shift registers.	2	K1	CO3
17. Interpret the CPU performance equation.	2	K2	CO4
18. Summarize the two types of IEEE floating point precision format.	2	K2	CO4

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| 19. Show the steps to overcome the pipeline hazards. | 2 | K2 | CO5 |
| 20. Recall the challenges in parallel processing. | 2 | K1 | CO5 |
| 21. Compare Static RAM and Dynamic RAM. | 2 | K2 | CO6 |
| 22. How does the processor handle interrupt requests? | 2 | K1 | CO6 |

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

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| 23. a) | Solve the following function using Karnaugh map method and construct the circuit of the minimal expression using only NAND gates.
$F(A,B,C,D)=\Sigma m(1,2,3,5,9,12,14,15)+\Sigma d(4,8,11).$ | 11 | K3 | CO1 |
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| b) (i) | Construct the following Boolean expression into standard SOP form
$F=ABC+A'B'+ABC'D.$ | 6 | K3 | CO1 |
| (ii) | Solve the Boolean function $F=A+B'C$ in a sum of minterms (SOP). | 5 | K3 | CO1 |

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| 24. a) | Infer the Boolean function using 8: 1 multiplexer.
$F(A, B, C, D) = A'BD'+ACD+B'CD+A'C'D$ | 11 | K2 | CO2 |
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| b) | Interpret a full adder using 2 half adders with its necessary explanations and diagrams. | 11 | K2 | CO2 |
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| 25. a) | Discover a 3 bit synchronous up counter using JK flip flop with the help of state table and state diagram. | 11 | K4 | CO3 |
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| b) | Analyse the different types of shift registers with neat diagrams. | 11 | K4 | CO3 |
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| 26. a) | Interpret the need for addressing in a computer system? Illustrate the different MIPS addressing modes with suitable examples. | 11 | K2 | CO4 |
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| b) | Illustrate Booth's multiplication algorithm and multiply the following signed 2's complement numbers
i. (+13) x (-6)
ii. (-13) x (-6) | 11 | K2 | CO4 |
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| 27. a) | Explain the data path segment for arithmetic logic Instruction and memory reference instructions. | 11 | K2 | CO5 |
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| b) | Demonstrate in detail about Hardware Multithreading. | 11 | K2 | CO5 |
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| 28. a) | List the various mapping techniques associated with cache memories. | 11 | K4 | CO6 |
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| b) | Examine the principle of a DMA controller and its role in enhancing the system performance. | 11 | K4 | CO6 |
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