Reg. No.																

Question Paper Code	14090

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Electrical and Electronics Engineering

24EEPC304 – DIGITAL ELECTRONICS

Regulations - 2024

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The RTL (Resistor–Transistor Logic) family uses resistors and transistors to perform logic operations and is known for (a) High speed and low power (b) Low cost but high power dissipation (c) High noise margin (d) High integration density	1	K1	CO1
2.	Power dissipation of CMOS circuits is significantly lower than TTL because (a) Only leakage current flows in static state (b) Transistors operate in saturation (c) Input current is large (d) Load current dominates	1	K2	CO1
3.	According to DeMorgan's second theorem,the complement of a sum of variables is equal to (a) The sum of the complements (b) The product of the individual complements (c) The NAND of variables (d) The OR of complements	1	K2	CO2
4.	In Boolean simplification, reducing the number of literals leads to (a) Simplified circuit with fewer gates (b) Increased noise (c) Higher propagation delay (d) More power consumption	1	K3	CO2
5.	During BCD addition, if the sum exceeds 9, the circuit (a) Adds 6 (0110) for correction (b) Subtracts 1 (c) Resets output (d) Generates parity bit	1	K2	CO3
6.	Hazards in combinational circuits are mainly caused by (a) Unequal propagation delays through different logic paths (b) High input frequency (c) Power supply variation only (d) Unused inputs	1	K1	CO3
7.	In an edge-triggered flip-flop, the transition occurs (a) Only on rising or falling edge of the clock pulse (b) At both logic levels (c) During complete clock period (d) When reset is active	1	K2	CO4
8.	A Moore model sequential circuit has outputs that depend on (a) Only present state (b) Both input and state (c) Previous output (d) Clock frequency	1	K1	CO4
9.	The VHDL operator "when–else" is commonly used for (a) Multiplexer design and conditional signal assignment (b) Clock generation (c) Counter control (d) Memory declaration	1	K1	CO5
10.	The synchronization of red, yellow, and green signals in traffic control systems depends on (a) Sequential timers and counters (b) Operational amplifiers (c) Logic inverters (d) Analog filters	1	K2	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

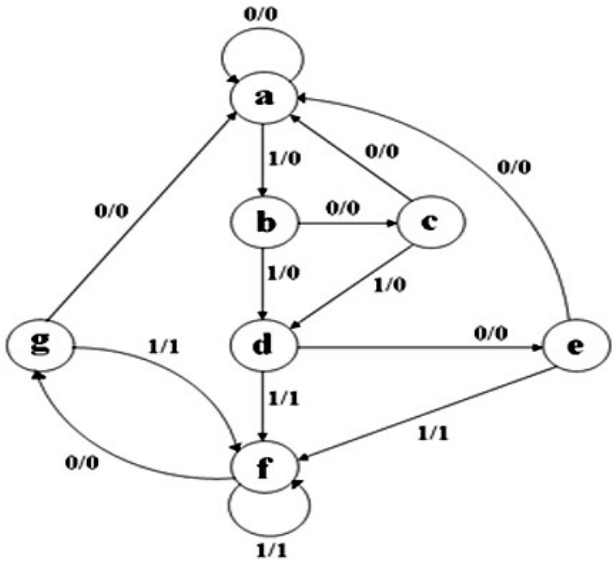
11.	Compare TTL and CMOS logic families in terms of power dissipation and speed.	2	K2	CO1
12.	Recall the reason why ECL does not saturate transistors during operation.	2	K1	CO1
13.	Name the universal gates in digital logic circuits.	2	K1	CO2
14.	Define Demorgan's theorem.	2	K1	CO2
15.	Compare borrow and carry in binary operations.	2	K2	CO3

16.	Outline the term Dynamic Hazard in digital logic circuits.		2	K2	CO3
17.	How many flip-flops are required to build a binary counter that counts from 0 to 7?		2	K2	CO4
18.	List any four applications of Flip flop.		2	K2	CO4
19.	Infer the term programmable logic array? Analyze how it differs from ROM?		2	K2	CO5
20.	List the various operators of VHDL.		2	K1	CO5
21.	Identify the digital component is used for counting time intervals in a stopwatch?		2	K3	CO6
22.	Identify the parameter that determines the signal-change timing in a digital traffic light controller.		2	K3	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Explain TTL NAND gate and explain its working with a neat diagram.	11	K2	CO1
		OR			
	b)	Compare the characteristics and performance of TTL, CMOS, and ECL logic families in terms of speed, power consumption, and noise immunity. Suggest suitable applications for each family.	11	K2	CO1
24.	a)	Identify and Minimize the following logic function using K-maps. Also realize using NAND gates. F(A,B,C,D) = ∑m(1,3,5,8,9,11,15)+d(2,13)	11	K3	CO2
		OR			
	b)	F(A,B,C,D)= ∑m(7,13,14,15)+ ∑d(2,5,12) Develop K-Map and implement the function using logic diagram.	11	K3	CO2
25.	a)	Develop the circuit that implements an 8-to-3 binary encoder with neat diagram.	11	K3	CO3
		OR			
	b)	Develop a full adder using two half adders.	11	K3	CO3
26.	a)	Analyze state reduction if possible after designing a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible.	11	K4	CO4



OR

	b)	Analyse the 4-bit SISO, SIPO, PISO and PIPO shift registers and explain its waveforms.	11	K4	CO4

27.	a)	Experiment with the design of BCD to Excess 3 code converter using PLA. Illustrate the design detail along with the PLA program table?	*11*	*K3*	*CO5*
		OR			
	b) (i)	Build data flow modeling style in VHDL to code for 4:1 multiplexer along with detailed explanation.	*06*	*K3*	*CO5*
	(ii)	Construct dataflow modeling in VHDL to describe 1:4 de-multiplexer in detail.	*05*	*K3*	*CO5*
28.	a)	A college canteen plans to automate its snack vending process, where customers insert coins and select an item from three available options. Develop a digital logic circuit for an automatic vending machine that dispenses one of three items based on coin input and selection switch. Develop the truth table, state transition diagram, and circuit implementation using flip-flops and logic gates.	*11*	*K3*	*CO6*
		OR			
	b)	In a manufacturing plant, a conveyor belt system is used to automatically sort products based on size and colour using digital sensors. Construct a digital control system for the industrial automation process (conveyor belt sorting). Develop the block diagram, sensor logic, and control sequence using logic circuits.	*11*	*K3*	*CO6*