Reg. No.																

Question Paper Code	14677

B.E. / B.Tech. - DEGREE EXAMINATIONS, APRIL / MAY 2026

Third Semester

Electronics and Instrumentation Engineering

24EIPC303 - DIGITAL SYSTEM DESIGN AND APPLICATIONS

Regulations - 2024

Duration: 3 Hours | Max. Marks: 100

PART – A (i) (MCQ)
(16 × 1 = 16 Marks)
Answer ALL Questions

		Marks	K – Level	CO
1.	Which number system uses base 2?	1	K1	CO1
	a) Decimal b) Binary			
	c) Octal d) Hexadecimal			
2.	SOP stands for	1	K1	CO1
	a) Sum of Products b) Series of Products			
	c) Sum of Powers d) None			
3.	Parity bit is used for	1	K1	CO1
	a) Compression b) Error detection			
	c) Encoding d) Multiplexing			
4.	Which logic family has the highest speed?	1	K1	CO2
	a) RTL b) TTL			
	c) ECL d) CMOS			
5.	CMOS stands for	1	K1	CO2
	a) Complementary MOS b) Current MOS			
	c) Controlled MOS d) None			
6.	TTL uses which component?	1	K1	CO2
	a) FET b) BJT			
	c) MOSFET d) Diode			
7.	Full adder adds	1	K1	CO3
	a) 2 bits b) 3 bits			
	c) 4 bits d) 1 bit			
8.	Multiplexer selects	1	K1	CO3
	a) One input b) Multiple outputs			
	c) One output d) None			
9.	Decoder converts	1	K1	CO3
	a) Binary to decimal b) Analog to digital			
	c) Digital to analog d) None			
10.	Flip-flop is	1	K1	CO4
	a) Combinational circuit b) Sequential circuit			
	c) Analog circuit d) Linear circuit			
11.	JK flip-flop removes	1	K2	CO4
	a) Race condition b) Indeterminacy			
	c) Feedback d) Delay			

12.	Counter counts		1	K2	CO4
	a) Pulses	b) Voltage			
	c) Current	d) Power			
13.	Hazard occurs due to		1	K2	CO5
	a) Delay	b) Noise			
	c) Timing issues	d) All			
14.	Race condition affects		1	K2	CO5
	a) Speed	b) Output			
	c) Stability	d) Power			
15.	FPGA is		1	K2	CO6
	a) Fixed logic	b) Programmable			
	c) Analog	d) Mechanical			
16.	PLA consists of		1	K2	CO6
	a) AND-OR arrays	b) OR-AND arrays			
	c) XOR arrays	d) None			

PART – A (ii) (Short Answer Questions)
(6 × 3 = 18 Marks)
Answer ALL Questions

17.	Explain SOP and POS forms.	3	K2	CO1
18.	Compare TTL and CMOS.	3	K2	CO2
19.	Explain the working of a Multiplexer (MUX) with a suitable block diagram and truth table.	3	K2	CO3
20.	Illustrate the operation of a flip-flop with a suitable diagram and describe its role in digital circuits.	3	K3	CO4
21.	Demonstrate how hazards occur in digital circuits with a suitable example.	3	K3	CO5
22.	Illustrate the architecture and working of an FPGA in digital system design.	3	K3	CO6

PART - B (Descriptive Answer Questions)
(6 × 11 = 66 Marks)
Answer ALL Questions

23.	a)	Simplify Boolean expression using K-map $F(A,B,C,D) = \Sigma(1,3,5,7,9)$ and implement using logic gates.	11	K3	CO1
		OR			
	b)	Demonstrate the error detection process in Hamming code using parity bits with a suitable example.	11	K3	CO1
24.	a)	Illustrate the characteristics of the CMOS logic family and their significance in digital circuits.	11	K3	CO2
		OR			
	b)	Identify the comparisons between RTL, DTL, TTL and ECL logic families.	11	K3	CO2
25.	a)	Construct a 4-bit full adder using suitable logic gates and illustrate its operation.	11	K3	CO3
		OR			
	b)	Construct an 8:1 multiplexer and illustrate its operation using a suitable block diagram.	11	K3	CO3

26.	a)	Analyze the operation of a JK flip-flop using a suitable truth table and timing concept.	*11*	*K3*	*CO4*
		OR			
	b)	Develop a MOD-6 counter and analyze its counting sequence using a suitable circuit diagram.	*11*	*K3*	*CO4*
27.	a)	Identify the effects of race conditions and hazards in digital circuits with suitable examples.	*11*	*K3*	*CO5*
		OR			
	b)	Build an asynchronous circuit using a flow table and determine its state transitions.	*11*	*K3*	*CO5*
28.	a)	Apply the concept of Programmable Logic Array (PLA) architecture to describe its operation in digital systems.	*11*	*K3*	*CO6*
		OR			
	b)	Apply the concept of FPGA architecture to describe its working with a suitable block diagram and its applications in digital systems.	*11*	*K3*	*CO6*