Reg. No.																

Question Paper Code	14048

B.E. / B.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

Third Semester

Electronics and Instrumentation Engineering

24EIPC303 - DIGITAL SYSTEM DESIGN AND APPLICATIONS

Regulations - 2024

Duration: 3 Hours Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	The binary equivalent of hexadecimal "2F" is: (a) 00101110 (b) 00101111 (c) 00101011(d) 01001111	1	K1	CO1
2.	VHDL is used for: (a) Hardware design(b) Software design (c) Database (d) Simulation only	1	K1	CO1
3.	The typical logic levels for TTL family are: (a) 0V and 5V (b) -5V and 0V (c) 0V and 3.3V (d) 0V and 12V	1	K1	CO2
4.	CMOS stands for: (a) Complementary MOS (b) Combined MOS (c) Complex MOS (d) Complete MOS	1	K1	CO2
5.	Difference output of half subtractor is: (a) A XOR B (b) A XNOR B(c) A AND B (d) A + B	1	K1	CO3
6.	In VHDL, entity defines: (a) Input/Output ports (b) Internal behavior (c) Timing (d) Simulation	1	K1	CO3
7.	In a 4-bit ripple counter, what is the maximum count? (a)8 (b)15 (c)16 (d) 10	1	K1	CO4
8.	Which type of flip-flop is most suitable for shift register design? (a)JKflip-flop (b)Dflip-flop (c)SRflip-flop (d) T flip-flop	1	K1	CO4
9.	In asynchronous sequential circuits, the output depends on: (a)Presentinputonly (b)Presentstateonly (c)Presentinputandpreviousstate (d) Clock signal	1	K1	CO5
10.	CPLD stands for: (a) Complex Programmable Logic Device (b) Central Programmable Logic Device (b) Compact Programmable Logic Device (d) Composite Programmable Logic Device	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

		Marks	K – Level	CO
11.	Convert $(101101)_2$ to decimal form.	2	K2	CO1
12.	Mention the advantages of K-map method over Boolean algebra method.	2	K2	CO1
13.	Define a logic family.	2	K1	CO2
14.	What are code converters? Give examples.	2	K1	CO2
15.	What is a Full Subtractor? List its inputs and outputs.	2	K1	CO3
16.	Mention the main components of a VHDL program.	2	K1	CO3
17.	What is meant by edge triggering?	2	K1	CO4
18.	Define asynchronous counter. Give an example.	2	K1	CO4
19.	Differentiate between synchronous and asynchronous circuits.	2	K2	CO5
20.	What is the effect of a hazard on circuit output?	2	K1	CO5
21.	What is meant by logic cell in FPGA design?	2	K1	CO6
22.	Compare PLA and PAL.	2	K2	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Explain the principle of error detection and correction using parity bits. Illustrate with examples.	*11*	*K2*	*CO1*
		OR			
	b)	Simplify the following Boolean function for minimal SOP & POS form using K-map i) F (A, B, C, D) = Σ (0,1,2,5,8,9,10) ii) F (A, B, C, D) = π(1,3,5,7,12,13,14,15).	*11*	*K2*	*CO1*
24.	a)	Apply the knowledge on working principle of Emitter Coupled Logic (ECL) family and Discuss how its speed is improved compared to TTL.	*11*	*K3*	*CO2*
		OR			
	b)	Write and explain a VHDL program to implement basic logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR). Include entity and architecture blocks.	*11*	*K3*	*CO2*
25.	a)	Design an Half Adder and Full Adder circuits. Derive their logic expressions and explain how they can be implemented using logic gates.	*11*	*K3*	*CO3*
		OR			
	b)	Write and explain a VHDL program to implement a8 X 1 Multiplexer using Gate level and dataflow modeling. Include entity, architecture, and testbench description.	*11*	*K3*	*CO3*
26.	a)	A sequential circuit has two JK Flip-Flops A and B, one input (x) and one output (y). the Flip-Flop input functions are, JA= B+ x JB= A'+ x' KA= 1 KB= 1 and the circuit output function, Y= xA'B. a) Draw the logic diagram of the Mealy circuit, b) Tabulate the state table, c) Draw the state diagram.	*11*	*K3*	*CO4*
		OR			
	b)	Write a VHDL program for D flip flop and JK flip flop.Include entity, architecture, and testbench description.	*11*	*K3*	*CO4*
27.	a)	Discuss hazards and glitches in digital circuits. Illustrate static and dynamic hazards with examples.	*11*	*K3*	*CO5*
		OR			
	b)	Design Asynchronous sequential circuit with two input X and Y with one output Z. Whenever Y is 1 input X is transferred to Z. When Y is 0 the output does not changes for any other change in X.	*11*	*K3*	*CO5*
28.	a)	Implement the following boolean function using PAL W(A,B,C,D)=Σ(0,2,6,7,8,9,12,13) W(A,B,C,D)=Σ(0,2,6,7,8,9,12,13,14) W(A,B,C,D)=Σ(2,3,8,9,10,12,13) W(A,B,C,D)=Σ(1,3,4,6,9,12,14)	*11*	*K3*	*CO6*
		OR			
	b)	Compare CPLD and FPGA for industrial applications in terms of speed, cost, and complexity.	*11*	*K3*	*CO6*