Reg. No.															

Question Paper Code	14209

M.E. / M.Tech. - DEGREE EXAMINATIONS, NOV / DEC 2025

First Semester

M.E. - Computer Science and Engineering

(Common to Computer Science and Engineering (with Specialization in Networks))

24PCNPC101 - ADVANCED COMPUTER ARCHITECTURE

Regulations - 2024

Duration: 3 Hours | Max. Marks: 100

PART - A (MCQ) (10 × 1 = 10 Marks)

Answer ALL Questions

		Marks	K – Level	CO
1.	Tomasulo's algorithm is used for: (a) Register renaming (b) Branch prediction (c) Memory hierarchy (d) Cache optimization	1	K1	CO1
2.	The main limitation of Instruction Level Parallelism (ILP) is: (a) Increased clock speed (b) Dependency between instructions (c) Large memory (d) Multithreading overhead	1	K1	CO1
3.	The principle of locality refers to: (a) Sequential instruction fetch (b) Data reuse in memory (c) Random data access (d) Hardware parallelism	1	K1	CO2
4.	Superscalar processors improve performance by: (a) Issuing multiple instructions per clock cycle (b) Reducing branch delay (c) Increasing memory size (d) Decreasing bus width	1	K1	CO2
5.	Distributed shared memory is used to (a) Reduce local cache (b) Share data among processors (c) Manage I/O operations (d) Control instruction flow	1	K1	CO3
6.	The main challenge in parallel processing is (a) Heat dissipation (b) Synchronization and consistency (c) Reduced power (d) Cost of memory	1	K1	CO3
7.	Google File System is primarily designed for (a) Local file storage (b) Large-scale distributed storage (c) Mobile apps (d) IoT systems	1	K1	CO4
8.	Power Usage Effectiveness (PUE) measures (a) CPU efficiency (b) Memory utilization (c) Data center energy efficiency (d) Network throughput	1	K1	CO4
9.	The term "Thread Block" is related to (a) CPU pipeline (b) GPU programming (c) Cache optimization (d) Virtual memory	1	K1	CO5
10.	GPU differs from CPU mainly in: (a) Memory type (b) Number of cores and parallelism (c) Cache size (d) Instruction set	1	K1	CO6

PART - B (12 × 2 = 24 Marks)

Answer ALL Questions

11.	What is Dynamic Scheduling?	2	K1	CO1
12.	What are the challenges in exposing instruction level parallelism?	2	K1	CO1
13.	List the advantages of Multicore processors.	2	K1	CO2
14.	Define dependency and list its types.	2	K1	CO2
15.	Recall any two important hurdles which make parallel processing challenging.	2	K1	CO3
16.	Differentiate Buses from crossbar networks.	2	K2	CO3

17.	Compare SMT and CMP.	2	K2	CO4
18.	Classify the elements of Interconnect Bus.	2	K2	CO4
19.	What is the purpose of the vector length register?	2	K1	CO5
20.	Define SIMD and give one real-time application example.	2	K1	CO5
21.	State the purpose of using multiple lanes in vector architecture.	2	K1	CO6
22.	What is the role of memory banks in vector processors?	2	K1	CO6

PART - C (6 × 11 = 66 Marks)

Answer ALL Questions

23.	a)	Define speculation and demonstrate hardware based speculation for executing a FOR LOOP.	11	K2	CO1
		OR			
	b)	Discuss how branch penalties can be minimized in pipelined architectures using dynamic hardware branch prediction techniques.	11	K2	CO1
24.	a)	Explain cache hit time reduction techniques and demonstrate their effectiveness in improving system performance.	11	K2	CO2
		OR			
	b)	Infer the concept of memory hierarchy to find data access patterns and also show how hierarchical organization improves performance.	11	K2	CO2
25.	a)	Discuss the application of basic coherence enforcement schemes in maintaining data consistency among processors.	11	K2	CO3
		OR			
	b)	Explain the working of multistage interconnection networks and design dimensions to optimize interprocessor communication performance.	11	K2	CO3
26.	a)	Build the architecture of warehouse-scale computers and discuss its design principles to relate physical infrastructure choices with operational cost efficiency.	11	K3	CO4
		OR			
	b)	Apply the principles of cell architecture to illustrate how bus design influences communication and performance among its processing elements.	11	K3	CO4
27.	a)	Explain the concept of vector processing to improve the performance of a processor compared to scalar execution using suitable examples.	11	K2	CO5
		OR			
	b)	Discuss how instruction-level parallelism is achieved in SIMD architecture for multimedia operations.	11	K2	CO5
28.	a)	Demonstrate the techniques used in eliminating dependent computations and state how they enhance vector performance.	11	K2	CO6
		OR			
	b)	Illustrate the working of roofline performance model and find its computational efficiency, memory bandwidth limitations.	11	K2	CO6